Model 4100

Boxcar Averager System

Instruction Manual
220518-A-MNL-D

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This product has been designed in conformance with the following IEC/EN standards:

EMC:	BS EN55011 (1991) Group 1, Class A (CSPIR 11:1990)	
	BS EN50082-1 (1992):	
		IEC 801-2:1991
		IEC 801-3:1994
		IEC 801-4:1988
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Introduction

Chapter 1

1.1 Introduction

This manual gives detailed instructions for setting up and operating ***SIGNAL RECOVERY*** Model 4100 Boxcar Averager Systems. It is split into the following chapters:-

Chapter 1 - Introduction
Provides an introduction to the manual, briefly describes what a boxcar averager is and the types of measurements it may be used for, and lists the major specifications of systems assembled from model 4100 series components.

Chapter 2 - Model 4121B Boxcar Averager
Describes how the model 4121B operates, details the connectors and controls on its front and rear panels and gives operating instructions for this single-channel boxcar averager module.

Chapter 3 - Model 4161A Dual Channel ADC & Display Module
Describes the connectors and controls on the model 4161A's front and rear panels, gives information on how to configure its RS232 and GPIB computer interfaces and details the computer commands that it responds to. There are also some notes to assist in developing software to control this module, as well as outline listings of typical programs.

Chapter 4 - System Configuration Guide
Describes how to assemble and interconnect typical systems using components from the 4100 series.

Appendix A
Gives the detailed specifications of the model 4121B and 4161A units.

New users are recommended to unpack the instrument(s) and in the case of the model 4121B carry out the procedure listed in chapter 3 to check that it is working satisfactorily. They should then read the whole manual before using the information in chapter 4 as a guide to assembling the required system.

1.2 What is a Boxcar Averager?

The boxcar averager is a specialized form of sample and hold circuit. Unlike most such circuits, it has the ability to integrate the voltage applied to its input for the duration of a gate pulse that it in turn generates on receipt of an external trigger. This trigger is synchronous with the signal. The gate pulse width and delay is adjustable allowing the gate to be positioned on the feature of interest. After each trigger, the boxcar outputs an analog voltage proportional to the integrated input signal.

The effect of the integration is to remove random fluctuations, or noise, from the signal for the duration of the gate. In addition, the fact that the boxcar does not respond to input signals except for the duration of the gate allows it to ignore background noise except when it is measuring a signal.

Usually the input signal is repetitive. In this case further signal to noise ratio improvement can be obtained by averaging the individual integrated sample voltages. The 4121B boxcar averager module includes an output averager to allow this to be done.

Boxcar averagers are particularly suitable for recovering signals from noise when the signal mark:space ratio is small (e.g. a pulse of a few tens of nanoseconds repeated at a few hundred hertz) and can be used both for static gate work, when the output is simply the amplitude of a particular feature on a pulsed signal, or for waveform recovery, where the pulse waveform is recorded. This capability has led to their use in many fields of scientific research including optics, electrochemistry and fundamental physics.

1.3 Key Specifications

The ***SIGNAL RECOVERY*** Model 4100 series consists of two modules suitable for assembling low cost boxcar averager systems featuring ease of operation and high performance. Systems can consist of one to four samplers, one or two display and ADC modules with GPIB and RS232 interfaces, and a full-width NIM bin and power supply to power and house these items. A separate four channel model 9650A digital delay generator can also be added for further flexibility, and the complete system can be controlled either manually from the front-panel controls or via the computer interfaces using either user-developed software or the free LabVIEW driver software.

Key specifications of systems assembled from model 4100 components include:

- 1.5 ns gate width
- 50 Ω DC and 1 MΩ AC or DC inputs
- 450 MHz Input Bandwidth
- 20 ns Trigger to Sample Delay
- 80 kHz Maximum Trigger Rate
- Analog or Digital Delay
- Last Sample Output & Samples Averaged Output
- Baseline sampling
- Linear or Exponential Averaging
- 20 mV Sensitivity

Model 4121B
Boxcar Averager

2.1 Introduction

The model 4121B is a low-cost NIM (Nuclear Instrumentation Module) unit that integrates the applied input signal over a predefined gate width starting at a predefined delay after an applied trigger. Each of these integrated samples of input signal can then be averaged, either within the 4121B using its own output averager, or in an associated computer following digitization as can, for example, be provided by the model 4161A (see chapter 3).

If the noise accompanying the signal is random, but the signal is repetitive and synchronous with the applied trigger, then the effect of the averaging is to improve the measured signal to noise ratio. With n triggers, the improvement obtained is $\sqrt{n}$

Static Gate Mode

When used on its own, the 4121B operates in the static gate mode, whereby the signal is sampled at the same point in time relative to the trigger for each trigger. Figure 2-1 shows the principle of this operating mode.

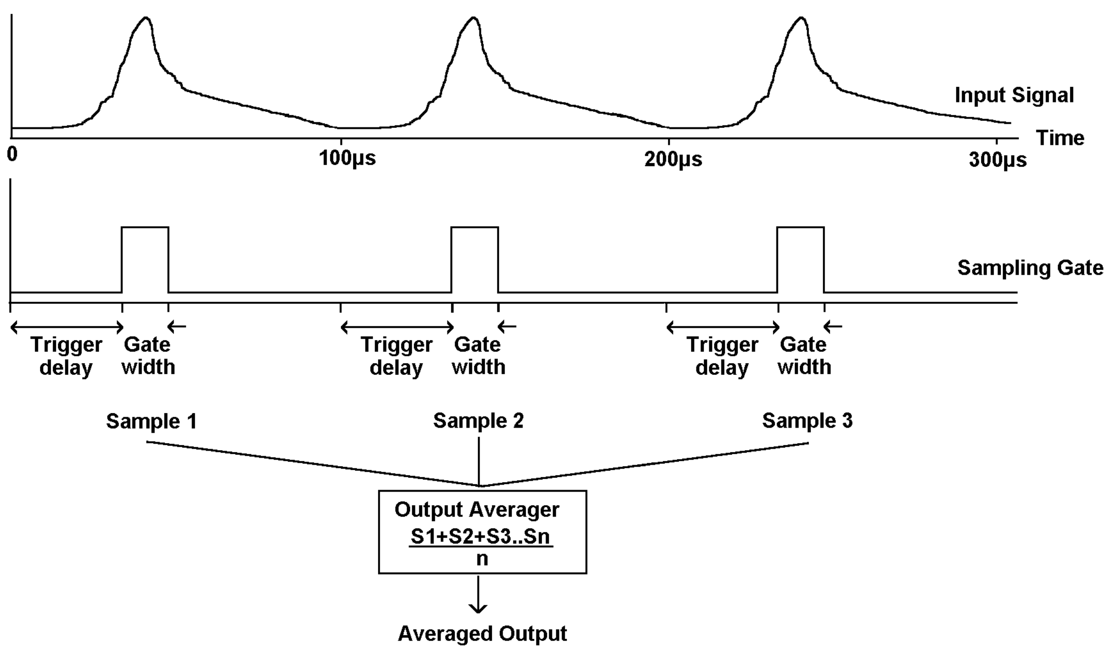

Figure 2-1, Static Gate Boxcar Averager with Linear Output Averaging

The signal is a repetitive, but noisy, pulse occurring at a regular time after each trigger, and the required information is the amplitude of the pulse. In order to measure this the 4121B's **GATE WIDTH** control is set to match the pulse width and the trigger **DELAY** control is set so that the gate width starts at the point that the pulse starts.

Each sample integral generates a value that appears as an analog voltage at the **LSO** (last sample output). In addition, however, this sample is fed into the output averager which in this example is set to the linear averaging mode.

Operating the boxcar then consists of resetting the output averager using the front-panel push button, starting the experiment and running it until the desired number of triggers have occurred, and then reading the averaged output by measuring the voltage at the **AVG** BNC connector using a voltmeter or ADC.

Waveform Recovery Mode
In conjunction with other equipment the 4121B can be used for waveform recovery. In this mode, the gate width is set to the required measuring resolution and is then "swept" on successive triggers or groups of triggers across the range of signal waveform to be recovered. Figure 2-2 shows the principle of this operating mode.

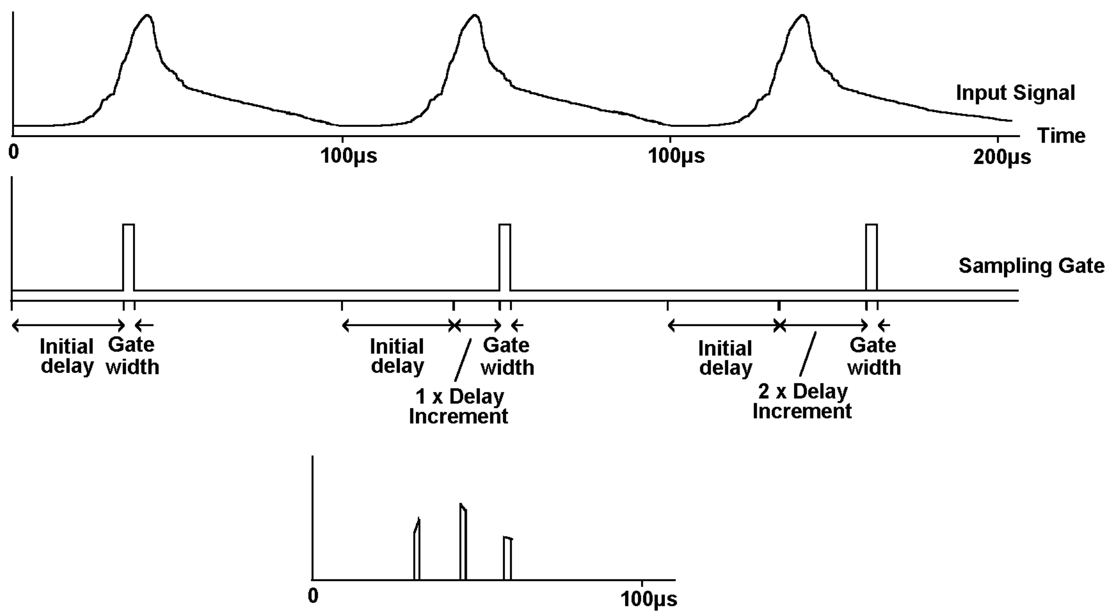

Figure 2-2, Waveform Recovery Boxcar Averager with Linear Output Averaging

As with the static gate example, the signal is a repetitive, but noisy, pulse occurring at a regular time after each trigger. This time, however, the required information is the waveform of the pulse. In order to record this, the system is configured so that the sampling gate position can be swept on successive triggers from an initial delay to a final delay which is equal to the initial delay plus p delay increments. It will be seen, therefore, that to recover a waveform over a period of time t the required number of increments p will be such that

$p = t/(\text{Delay Increment})$.

As before, each trigger generates a last sample output, and in the bottom diagram of figure 2-2 the three resulting samples from the three triggers shown are plotted as pulses. Clearly, if the delay increment is made smaller, ideally the same as the gate width, then the resulting group of pulses will merge to give an overall waveform equivalent to the input signal waveform.

The above description assumes no output averaging. In order to add this function, the system needs to keep the gate delay fixed at a given position and then take many samples and average them before moving on to the next position. Practically, this means that the output is taken from the 4121B's **AVG** output instead of the **LSO** output, and that the averager is set to the exponential mode, which eliminates the need to reset it after each group of triggers.

There are various methods by which the gate delay can be swept and the resulting waveform recorded. Historically, boxcar averagers used in waveform recovery mode employed analog chart recorders to record the output as the gate delay was adjusted. Such a system can still be assembled using the 4121B by applying a ramp voltage to the 4121B's internal voltage controlled trigger delay and to the X-axis of the chart recorder, with the Y-axis input connected to the 4121B's **AVG** output. The ramp voltage may take the form of a staircase waveform, in which case the averager samples and averages for the number of triggers occurring during each step of the staircase, or it may simply be a linear ramp. In both cases, good results are obtained as long as the number of samples to average is typically at least ten times smaller than the number of triggers available within the time by which the gate delay changes by a time equal to the gate width setting.

In modern systems, the chart recorder is replaced by an ADC and computer. The gate delay can still be adjusted using the analog delay control of the 4121B, or more precise control may be achieved using an external digital delay generator, such as the ***SIGNAL RECOVERY*** model 9650A. Two possible 4121B waveform-recovery systems are therefore:-

4121B with Analog Gate Delay Control

A general purpose analog signal to PC interface card such as one of those available from National Instruments and other vendors is used to provide an analog control voltage to the 4121B's internal voltage controlled adjustable delay. The same card is also used to digitize the resulting signal at the 4121B's **LSO** or **AVG** outputs. User-developed software is used to control the delay and record the resulting output signal. Note, however, that ***SIGNAL RECOVERY*** do not supply suitable interface cards and software.

4121B with Digital Gate Delay Control

This system uses a ***SIGNAL RECOVERY*** model 9650A to provide precise and computer-adjustable delayed triggers to the 4121B, with the latter's internal trigger delay generator being bypassed. The resulting signal at the 4121B's **LSO** or **AVG** outputs is digitized using the model 4161A dual channel ADC and control module (see chapter 3) with the whole system controlled from the LabVIEW development environment using the user's copy of LabVIEW and the free drivers available from ***SIGNAL RECOVERY***. Alternatively the user may develop his own software using whatever language he chooses.

2.2 Installation

2.2.01 Inspection

Upon receipt the model 4121B Boxcar Averager should be inspected for shipping damage. If any is noted, ***SIGNAL RECOVERY*** should be notified immediately and a claim filed with the carrier. The shipping container should be saved for inspection by the carrier.

2.2.02 NIM BIN Requirements

The model 4121B Boxcar Averager is a standard double-width Nuclear Instrument Module (NIM). It requires a bin that fully conforms to the NIM standard. ***SIGNAL RECOVERY*** offer various bin options, but perhaps the most commonly used one for assembling model 4100 systems is the 4001A/4002D combination of bin and power supply. This bin allows up to four 4121B boxcar averager and two 4161A dual channel ADC modules to be accommodated and powered.

2.2.03 Grounding

The 4121B's chassis is internally returned to the third wire or grounding pin of the bin's input power connector. For equipment and operator safety, it is important that this grounding pin be returned to a good earth-ground connection via the ground wire of the power distribution system. This precaution serves to prevent shock hazards.

2.2.04 Ventilation

A standard NIM bin does not have forced air ventilation, and the model 4121B has no special ventilation requirements.

2.3 Front Panel

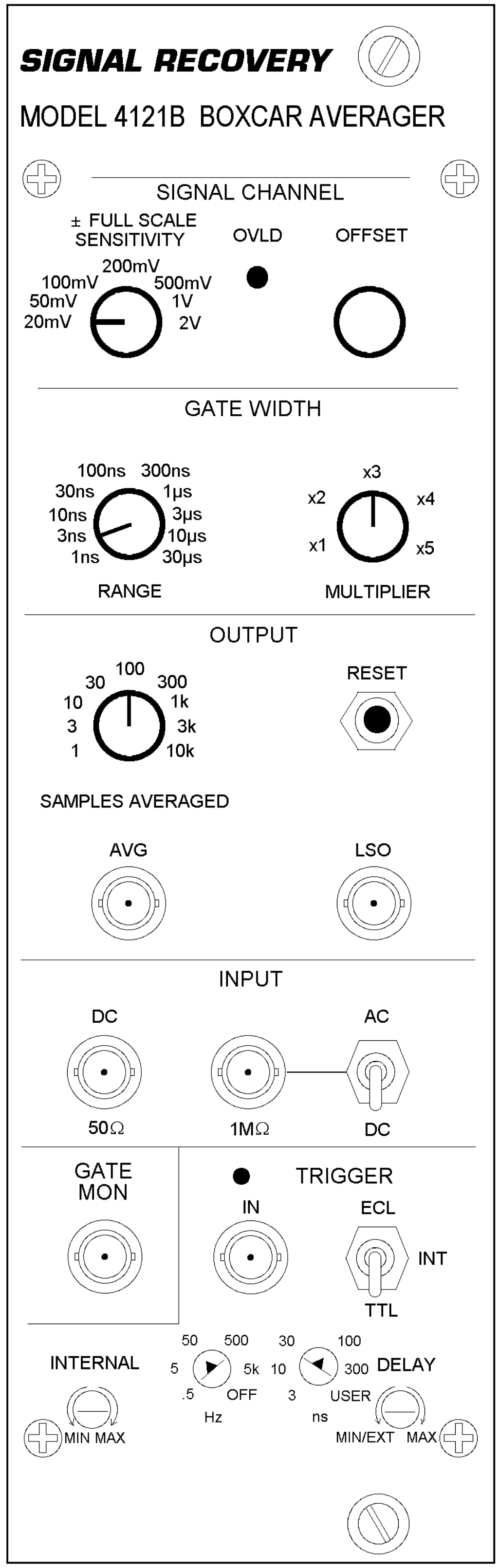

Figure 2-1, Model 4121B Front Panel

As will be seen from figure 2-1, there are five rotary switches, four rotary controls, two toggle switches, one push-button switch, five BNC connectors and two LEDs on the model 4121B front panel. The purpose of each of these items is discussed in the following sections.

2.3.01 Signal Channel Controls & Indicator

The **SENSITIVITY** rotary switch, **OFFSET** control, and **OVLD** indicator are located in this section of the panel.

The **SENSITIVITY** switch is used to select any one of seven different full-scale sensitivities ranging from ±20 mV to ±2 V in a 1-2-5 sequence. A full-scale synchronous signal will give ±10 V out at the **LSO** and **AVG** outputs (exponential averaging; fully converged).

The ten-turn **OFFSET** control sets the level of DC offset from an internal source that is added to the applied signal. It can be used to null offset on the applied signal or to compensate for stray internal drift and offset.

The range of the offset with respect to the input is a function of the selected full-scale sensitivity, as follows:-

Sensitivity	Offset
20 mV - 200 mV	±10 × FS
500 mV - 2 V	±2 V

Maximum negative offset occurs with the dial fully counter clockwise and maximum positive offset when it is fully clockwise. Zero is at nominally five turns from either extreme. Note that the 4121B must be triggering for the effect of the offset setting to be seen at the output.

The **OVLD** (overload) indicator will light for a minimum of 0.1 s at any time that the applied input exceeds ±2.2 V or the output exceeds ±10 V. Under conditions of permanent overload it remains lit.

2.3.02 Gate Width Controls

The 4121B's gate width, or sampling duration, is set by the product of the **RANGE** switch setting and the **MULTIPLIER** setting. The **RANGE** switch has settings from 1 ns to 30 µs, while the range of the **MULTIPLIER** control, a one-turn dial, extends this from ×1 to ×5. Hence the total gate-width setting range extends from 1 ns to 150 µs.

An analog signal representing the gate pulse is provided at the **GATE MON** output connector, allowing the use of an oscilloscope to determine the precise duration and timing of the gate opening. The monitor pulse is 0.3 V (into 50 Ω to ground) and its width is equal to the gate width. There is, however, a small intrinsic delay between the actual gate opening and the monitor pulse. This delay does not exceed 5 ns when the **GATE MON** output is loaded with 50 Ω.

2.3.03 Output Controls

This area of the panel contains the **SAMPLES AVERAGED** switch, the **RESET** pushbutton, and the two output BNC connectors, **AVG** and **LSO**.

The **SAMPLES AVERAGED** switch provides settings from 1 to 10,000 in 1-3-10 sequence. The significance of this parameter depends on whether the 4121B is set to exponential or linear averaging, as set by the position of an internal jumper (see section 2.5.02).

If set to exponential averaging, the setting defines the number of samples of which the output is the RC weighted average after nominally five times the selected number of samples have occurred. When the number of samples taken equals the switch setting, the output will be at 63% of its final value. The number of samples required to converge within 1% of the final value is five times the switch setting.

For example, if the **SAMPLES AVERAGED** switch were set to 100 with a full-scale signal applied, the 4121B's output would reach 6.3 V after 100 samples and 10 V after 500 samples. At that point the Signal-to-Noise Improvement Ratio (SNIR) would be 10 ($\sqrt{100} = 10$). If the number of samples taken, n, is less than five times the setting, the SNIR will be less than $\sqrt{n}$. Taking more than $5n$ samples provides no further improvement in SNIR.

If set to the linear averaging mode, full-scale output occurs when the number of samples taken is 67% of the number selected by the **SAMPLES AVERAGED** switch, with the exception that on the 1, 10, and 100 ranges, full-scale output occurs when the number of samples equals the number selected by the **SAMPLES AVERAGED** switch. Independent of the **SAMPLES AVERAGED** switch setting, when linear averaging, the output is always the sum of the number of samples taken. The SNIR equals the square root of the number of samples taken.

Pressing the **RESEST** pushbutton resets the integrator, establishing a zero output. The integrator can also be reset by applying a TTL logic 0 to the rear-panel **RESET** connector.

In linear averaging, all samples are summed so that, for a given input, the output level increases with each sample taken. This increase in output level doesn't stop until output overload occurs. The reset function provides the only way of restoring zero output, and is normally done at end of each run.

In exponential averaging, the output approaches final convergence asymptotically. As a result, providing the input signal is less than full scale, output overload does not occur and there is no need to use the reset capability.

The averager output is provided at the **AVG** BNC connector. Full-scale output is ±10 V and the output impedance is 50 Ω with the constraint that the load impedance must be larger than 2 kΩ.

The integral of the last (i.e. most recent) sample taken appears at the **LSO** (last sample output) BNC connector. Maximum output is ±10 V. The output impedance is 50 Ω with the constraint that the load impedance must be larger than 2 kΩ. This output defines the last (most recent) sample, that is, the average input level for the duration of the most recent gate opening. It is provided for both signal and baseline samples. Because it is taken from the input to the output averager, it is not affected in any way by the setting of the **SAMPLES AVERAGED** switch or the averaging mode.

In a typical 4100 system using the 4161A ADC module, the **LSO** output of a 4121B is cabled to the **CHN A** input of a 4161A. Similarly, the **LSO** output of a second 4121B can be cabled to the **CHN B** input of the 4161A.

2.3.04 Input Connectors & Coupling Selector Switch

The two signal input connectors and the coupling toggle switch are located in this section of the panel. Although both inputs are active at all times, in normal use only one input is used at any one time.

The connector marked **50 Ω** provides a 50 Ω input impedance and is always DC coupled, while that marked **1M Ω** provides a 1M Ω input impedance that can be either AC or DC coupled as selected by the adjacent coupling switch.

2.3.05 Gate Monitor Output

As described above in section 2.3.02, the signal at the **GATE MON** output provides a marker pulse (0.3 V into 50 Ω) that defines the time position and duration of the gate opening. It lags the actual gate opening by no more than 5 ns.

2.3.06 Trigger Input, Internal Oscillator and Delay Controls

In addition to the trigger input connector, this section contains the trigger indicator, the trigger mode toggle switch, the internal oscillator frequency setting controls, and the trigger delay setting controls.

In the external trigger mode, a sample is taken each time a trigger is applied to the trigger input connector, marked **IN**. The actual trigger polarity and impedance is set by the adjacent toggle switch.

When the switch is set to **ECL**, the input impedance is 50 Ω returned to -2 V and the trigger source must develop ECL levels into this impedance. When it is set to **TTL** it is suitable for TTL signals. Hence it should be set to match the type of trigger source. Both TTL and ECL triggering takes place on the rising edge of the applied trigger, with the restriction that an ECL trigger must be at least 4 ns wide and a TTL trigger must be at least 15 ns wide.

If the trigger mode toggle switch is set to **INT**, the 4121B is triggered by its own internal oscillator. The oscillator's output also appears at the rear-panel **INT OSC OUT (TTL)** connector so that it is available for triggering the experiment.

Each time the 4121B is triggered, either internally or externally, the triggered LED lights for at least 0.1 s. At rapid trigger rates, the LED appears to glow steadily.

The maximum trigger rate for which every trigger is processed in the external trigger mode is nominally 80 kHz, unless baseline sampling is selected, in which case the maximum trigger rate is 20 kHz. Higher trigger rates can be applied but in this case some triggers will be ignored, since triggers applied while the 4121B is still executing its response to the previous trigger are not processed. The **BUSY OUT (TTL)** signal provided at a rear-panel connector is asserted (i.e. set to a TTL high logic level) when processing of the sample initiated by the previous trigger is complete and the 4121B is trigger receptive again.

When using the internal oscillator, the two **INTERNAL** controls at the lower left corner of the front panel are used to set the oscillator frequency. These controls, which are screwdriver adjustable, consist of a range switch and a vernier. The range switch, marked **Hz**, has six positions. Each position (other than **OFF**, in which the oscillator is turned off), defines a frequency range. The actual oscillator frequency within the selected range is set by the adjacent multiplier, marked **MIN MAX**. The range for each position of the switch is as follows:

Setting	Nominal Range
.5	.5 Hz to 5 Hz
5	5 Hz to 50 Hz
50	50 Hz to 500 Hz
500	500 Hz to 5 kHz
5000	5 kHz to 40 kHz

The model 4121B includes a gate delay generator that is particularly useful in static gate operation for positioning the sample gate on the feature of interest. There are two screwdriver adjustable controls affecting this delay, consist of a range switch and a vernier marked **RANGE** and **DELAY** respectively. The gate delay generator is active in both external and internal trigger modes, unless it is bypassed by repositioning an internal jumper (see section 2.5.01).

The delay range switch, marked **RANGE**, has six positions, **3 ns**, **10 ns**, **30 ns**, **100 ns**, **300 ns**, and **USER**. Each position corresponds to the delay obtained if the associated vernier control marked **DELAY** is set to **MAX**. The **USER** setting is factory set to a delay range of 10 µs, but this delay can be changed by the user to settings of 1 µs, 10 µs, 100 µs, 1 ms or 3 ms by changing an internal capacitor (see section 2.5.03). When the **DELAY** control is set to the **MIN/EXT** position, the delay is the minimum possible for that range.

The delay is also affected by the voltage applied to the rear-panel **DELAY SCAN IN** BNC connector. The delay obtained by applying this voltage is calibrated when the **DELAY** control is set to **MIN/EXT**, in that an applied voltage of 0 V gives minimum (intrinsic) delay, while a voltage of +10 V gives a delay equal to the setting of the **RANGE** control. If a ramp voltage is applied, the delay linearly increases as the ramp advances from 0 V to +10 V.

NOTE: If the vernier is not set to MIN/EXT, the resulting delay is not calibrated with respect to the applied external voltage.

If the internal trigger delay generator is bypassed (see section 2.5.04) then the intrinsic delay of the 4121B is nominally 20 ns when using ECL triggering and 25 ns when using TTL triggering. This delay should be allowed for in the design of experiments.

In a 4100 system using the 9650A delay generator, the A and B outputs of the 9650A connect to the trigger **IN** inputs of the two model 4121B's, which are operated in the external **TTL** trigger mode. With this configuration, the gate delay is obtained via the 9650A by delaying the applied trigger to the 4121B.

2.4 Rear Panel

The rear panel of the 4121B, shown in figure 2-2, accommodates a toggle switch, six BNC sockets and the NIM standard power socket.

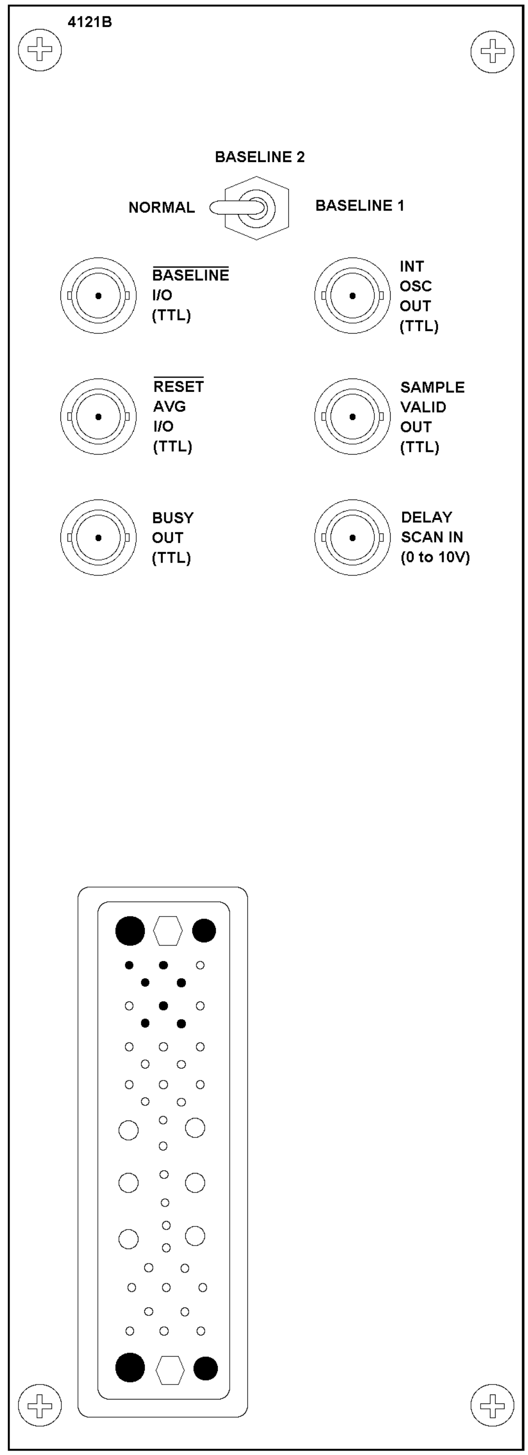

Figure 2-2, Model 4121B Rear Panel

2.4.01 Baseline Sampling Mode Switch

This switch has three positions, **NORMAL**, **BASELINE 1**, and **BASELINE 2**.

When it is set to **NORMAL**, samples are taken with respect to ground and every sample directly contributes to the averager output. This selection offers the advantage of the fastest possible trigger rate. The disadvantage of the **NORMAL** setting is that signal baseline shifts can cause corresponding output level shifts and so act as a source of error.

In the other two positions, samples do not contribute directly to the averager output. Instead, two samples are taken, one of the signal and the other of the baseline, and the difference is transferred to the averager. This technique compensates for baseline drift. The maximum error due to baseline drift is reduced to that which can occur between the time the signal sample is taken and the time the baseline sample is taken. Disadvantages of baseline sampling are that twice as many triggers are required to make a measurement and that the maximum trigger rate is reduced from 80 kHz (nominally) to 20 kHz.

Note that there is no provision in the 4121B for establishing a different value of delay for a baseline sample than that for a signal sample, so this has to be done externally by switching the trigger time between the baseline and signal delay values. Alternatively the signal and baseline samples can be taken at the same delay time but the experiment can be arranged such that the baseline sample corresponds to no signal at the detector. For example, in an optical experiment, a shutter or light chopper could be used to ensure that baseline samples are taken when the detector is masked from the signal while signal samples occur when it is exposed. The system described in section 4.2.03 is an example of such an experiment.

The 4121B makes configuring such experiments easier using the baseline I/O function, which operates as follows:-

BASELINE 1
In this mode, the **BASELINE I/O (TTL)** connector functions as a TTL output that reverses state with each trigger. The reversal occurs synchronously with the positive-going edge of a TTL or ECL trigger. If the **BASELINE I/O (TTL)** output is high when the sample is taken, it is a signal sample. If it is low, a baseline sample is taken. After the baseline sample is taken, the difference between the baseline sample and the preceding signal sample is applied to the averager. Hence the averager output is incremented every other trigger. The state of the **BASELINE I/O (TTL)** output can be sensed by peripheral apparatus either to switch the timing of the triggers or to drive a shutter or chopper so that baseline and signal samples are properly timed.

BASELINE 2
In this mode, the **BASELINE I/O (TTL)** connector functions as an input so that the experiment can directly control the sampling mode of the 4121B. When this input is high, the 4121B takes a signal sample. When this input is low, it takes a baseline sample and the difference between the baseline sample and the preceding signal sample is transferred to the averager.

2.4.02 BASELINE I/O (TTL) Connector

The operation of this input/output is described above in section 2.4.01

2.4.03 INT OSC OUT (TTL) Connector

The output of the internal trigger oscillator is provided at this connector and is present at any time that the front-panel **INTERNAL** frequency control, marked **Hz**, is set to any setting except **OFF**. It is not necessary that the trigger mode switch be set to **INT**. An internal jumper allows the 4121B to trigger on the positive-going or negative-going edge of the oscillator output (see section 2.5.05).

2.4.04 RESET AVG I/O (TTL) Connector

Applying a short to ground, from either an open-collector TTL output or via a relay contact or FET switch closure to this connector resets the 4121B's output averager and initializes its logic. Alternatively, pressing the front-panel **RESET** pushbutton causes a TTL logic 0 to be output to this connector. If the **RESET AVG I/O (TTL)** connectors on two or more 4421B's are connected together, pressing the **RESET** pushbutton on any one will reset them all.

NOTE: The reset must come from an open-collector or switch contact closure source because the resets are tied together. Even if the resets from other modules aren't connected to the common reset line, an appropriate source is necessary to accommodate the front-panel RESET pushbutton.

2.4.05 SAMPLE VALID OUT (TTL) Connector

This TTL output goes low whenever the 4121B is triggered. It remains low until the resulting sample is valid, when it goes high. Hence the rising edge of this signal can be used as a trigger to a following ADC, such as the 4161A (see chapter 3), indicating when the voltage at the 4121B's **LSO** front-panel output is valid.

In a typical 4100 system using the 4161A, the **SAMPLE VALID OUT (TTL)** output of the 4121B connects to the **CHN A ADC TRIGGER INPUT** of the 4161A. Similarly, if a second 4121B is used then its **SAMPLE VALID OUT (TTL)** output of the 4121B connects to the **CHN B ADC TRIGGER INPUT** of the 4161A.

2.4.06 BUSY OUT (TTL) Connector

The signal at this connector goes low (i.e. to logic 0) whenever the 4121B is triggered,, and remains there until the sampler is reset and the 4121B can be triggered again. In conjunction with trigger holdoff facilities that can, for example, be provided by the ***SIGNAL RECOVERY*** model 9650A digital delay generator, then this output allows the 4121B to prevent the generation of a new trigger until the data acquired by the present trigger has been processed.

2.4.07 DELAY SCAN IN (0 TO 10 V)Connector

The voltage applied to this connector determines the delay of the internal trigger delay generator front-panel **DELAY** vernier control is set to **MIN/EXT**. The delay can be varied from minimum (intrinsic delay) with 0 V applied (or with the connector left disconnected) to the value selected by the delay **RANGE** switch, when +10 V is applied.

2.4.08 NIM Power Connector

The power and ground connections are made via this connector, as follows.

Pin	Function
11	-6 V
17	-12 V
28	+24 V
29	-24 V
34	GROUND
16	+12 V
10	+6 V

2.5 Internal Adjustments

2.5.01 Introduction

The model 4121B has three internal jumper selections and an internal component selection that affect its operation. The following sections describe how to check, and if necessary change, these settings.

Each of these adjustments requires the unit to be withdrawn from the rack and for a cover to be removed, so the following instructions are common to all three.

1) Turn off the power to the NIM rack and remove the model 4121B.

2) Place the model 4121B on a flat surface so that the front panel of the module is closest to you and the top edge towards the left.

3) Remove the four Posidriv screws holding the cover in place.

4) The layout of the main board assembly is shown in figure 2-3, where the position of the jumpers J6 and J9 is clearly marked. Jumper J6, which is used to bypass the internal trigger delay generator, normally has a DIL header plug fitted with two coaxial cables plugged onto it. Jumper J9 is used to set the averaging mode.

5) A second board, the trigger delay board, is mounted along the bottom edge of the unit, which in this case is on the right. Most of the components on this board are located on the underside, but there is a capacitor towards the front panel soldered to two pins projecting from the top side. Figure 2-4 shows a side elevation of this board to aid identification. It is this capacitor that has to be changed to change the trigger delay range set by the **USER** setting of the **RANGE** control from the default value of 10 µs.

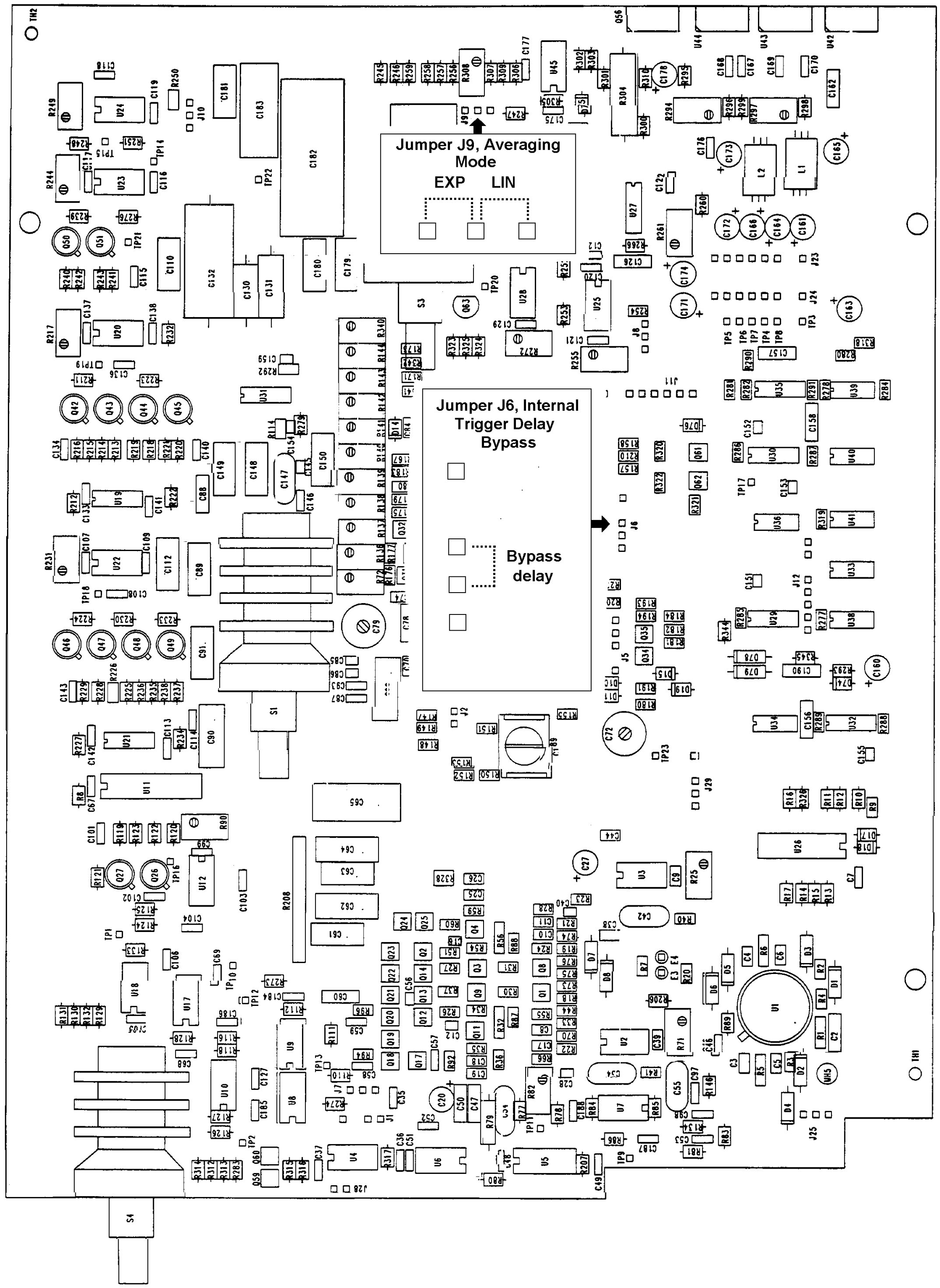

Figure 2-3, Model 4121B - Location of Internal Jumpers J6 and J9 on Main Board

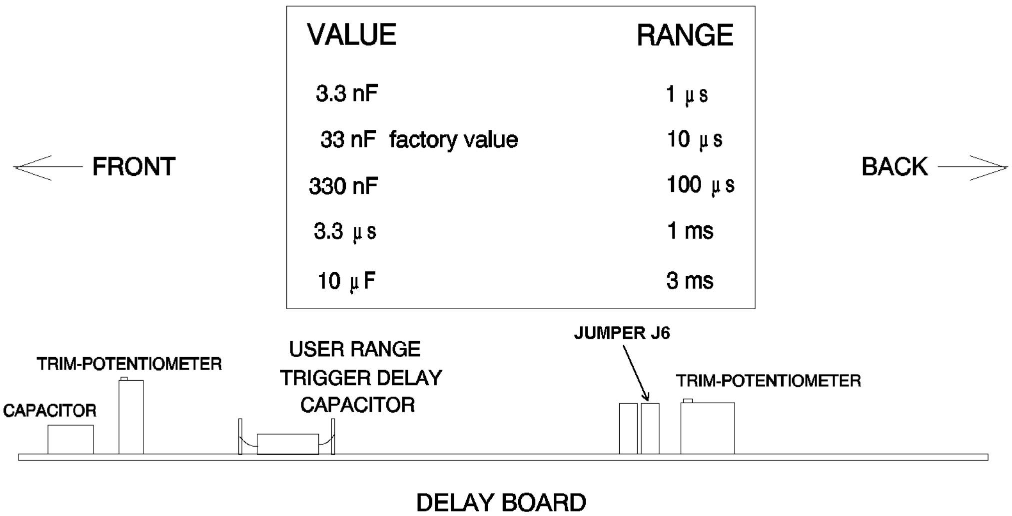

Figure 2-4, Model 4121B - Location of User Adjustable Trigger Delay Range Capacitor and Jumper J6 on Delay Board

6) Also mounted on the Delay Board is jumper J6 that is used to set the polarity of the internal oscillator output. The position of this jumper is highlighted in figure 2-4; it is towards the rear of the instrument.

7) Once the Averaging Mode, Oscillator Output Polarity, Trigger Delay Generator Bypass and/or Delay Range Capacitor have been set as required, replace the module cover removed earlier in this procedure and secure using the four Posidriv screws.

8) If any of the settings are changed from the factory default values, it will prove useful in the future to know what the settings are. Hence it is suggested that a self-adhesive label be applied to the unit giving the following information:

Averaging Mode	Linear or Exponential
Delay Generator	Bypassed or In-Circuit
Delay Range	Delay Range Capacitor and corresponding **USER** range
Oscillator Polarity	Positive or Negative

2.5.02 Linear/Exponential Output Averager Selection

The averaging mode of the 4121B's output averager is set by the position of jumper J9 on the main board, as shown in figure 2-3. When the front of the module is towards you, if the left-hand pair of pins is linked using the pin header then the averaging mode is exponential. This is the factory default. If the right-hand pair of pins is linked using the header then the averaging mode is linear.

2.5.03 Trigger Delay USER Setting Range Adjustment

The delay obtained from the internal trigger delay when its **RANGE** switch is set to the **USER** setting depends on the value of a capacitor mounted on the delay board. The default value of this capacitor, 33 nF, gives a maximum delay on the **USER** setting of 10 µs, but each model 4121B is shipped with a capacitor kit, part number 231034, that allows four other capacitor values to be fitted. Figure 2-4 shows the location of the capacitor on the delay board and the maximum delay for each value. The capacitor can be easily changed as required using conventional tools and a small soldering iron.

2.5.04 Trigger Delay Bypass

The internal trigger delay generator can be bypassed in order to minimize the intrinsic delay. In order to do this the DIL header plug fitted with two coaxial cables plugged onto it should first be removed from Jumper J6 on the main board (see figure 2-3). Next the two middle pins should be linked with a user-supplied 2-pin jumper. (Note that in this mode the internal oscillator cannot be used as a source of triggers, so the header from jumper J6 on the *delay board* can be removed and used to link the pins of J6 on the *main board*.)

2.5.05 Internal Oscillator Polarity

Jumper J6 on the *delay board* (figure 2-4) determines whether triggering will take place on the positive going or negative going edge of the internal trigger oscillator output. The detailed view of this jumper is shown in figure 2-5.

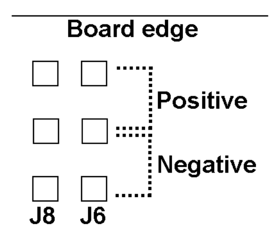

Figure 2-5, Model 4121B - Internal Oscillator Output Polarity Control - Delay Board

As can be seen, there are three pins. When pin 2 (center pin) is jumpered to pin 1 (pin closest to edge of board), triggering occurs on the positive-going edge. Jumpering pin 2 to pin 3 selects triggering on the negative-going edge.

2.6 Operation

2.6.01 Installation & Initial Checks

After installing the model 4121B in its bin, it is sensible to make some simple checks to verify that it is working properly. The following procedure allows such checks to be easily performed. To make these checks requires a sinewave oscillator capable of generating a 4 V pk-pk sinewave at 100 Hz into a 50 Ω load. This generator will provide the required input signal to the 4121B. An oscilloscope is also needed to observe the resulting 20 V pk-pk 100 Hz sinewave at the output of the 4121B. The procedure is as follows.

1) Set the controls on the 4121B as follows.
   Sensitivity Range: **2 V**
   Gate Width: **300 ns**, ×**5**
   Samples Averaged: **1**
   Trigger Mode: **INT**
   Trigger **INTERNAL** vernier: **MAX**
   Trigger Range: **5 K**

2) Set the signal generator to give an sinusoidal output of 4 V pk-pk into 50 Ω at 100 Hz, and connect this signal to **50 Ω** input of the 4121B.

3) Monitor the 4121B's **LSO** output with the oscilloscope. Set the oscilloscope controls to conveniently observe the 4121B output signal, which should be a 20 V pk-pk stepped approximation to a 100 Hz sine wave.

This completes the initial checks. If the given result was obtained one can be reasonably sure that the 4121B has not be subject to damage in transit and is working properly.

2.6.02 Connections

In a typical experiment, the input signal is connected to one of the two input connectors and a synchronous trigger is applied to the trigger **IN** connector. The **LSO** or **AVG** outputs are monitored using voltmeter or the model 4161A Dual ADC and Display Module, while the signal and the **GATE MON** output are typically monitored on an oscilloscope.

It is then a relatively straightforward job to adjust the trigger delay, using either the internal delay generator or an external delay, the full-scale sensitivity and offset controls, and the output averager controls to obtain the required output.

More sophisticated experiments may use the baseline sampling capability of the 4121B and/or its internal oscillator. One such system configuration is described in Chapter 4.

2.6.03 Sensitivity Control

The sensitivity should be set to give as near full-scale output as possible without overload. Since the maximum input that can be applied without overload is ±2 V for any sensitivity setting, if the signal is very noisy, it may be necessary to attenuate it ahead of the 4121B to avoid input overload. Offsets, both external and input, can be nulled using the ten-turn **OFFSET** control. Note, however, the unit must be triggering to see the effect of the adjustment.

2.6.04 Gate Width Control

The gate width sets the sample duration and hence the time resolution. The narrower the gate width, the finer the signal detail that can be recovered. However, delay jitter can be a significant resolution-limiting factor and its impact is generally greater, relatively speaking, with a narrow gate width than with a wide one.

NOTE: In systems using the SIGNAL RECOVERY model 9650A the delay jitter is generally set by the 9650A and not by the 4121B.

2.6.05 Output Averager Control

The **SAMPLES AVERAGED** switch directly sets the attainable signal to noise improvement ratio (SNIR) when set to exponential averaging. The higher the setting, the better the SNIR, but at the expense of increased experiment time. Unfortunately, whereas experiment time varies directly with the setting, SNIR varies with the square root of the setting, tempering the practicality of always operating with a high samples averaged setting.

If set to the linear averaging mode, the **SAMPLES AVERAGED** switch simply sets the number of full-scale input samples (67% of setting except on the 1, 10, and 100 ranges, where it is 100% of setting) needed to develop a full-scale output. It has no effect on SNIR.

Remember that baseline sampling doubles the number of triggers required because sample pairs are processed as opposed to individual samples.

The averager output is provided at the **AVG** connector and the most recent sample level at the **LSO** connector. The **RESET** button can be used to reset (zero) the averager at any time.

In an experiment where it is necessary to precisely know when the output has settled so that it can be processed, the rear-panel **SAMPLE VALID OUT (TTL)** output provides the required information. This output goes to logic 0 when the 4121B is triggered. It remains at logic 0 until any output change from the resulting sample has had time to stabilize, at which point it goes to logic 1. This positive-going transition can then be used to trigger an A/D converter.

2.6.06 Input

With a 50 Ω input impedance, there are no further input decisions to be made. On the other hand, if the input signal is connected to the 1 MΩ input, AC or DC coupling must be selected.

2.6.07 Triggering

To trigger internally select **INT** and then use the range and vernier controls to set the desired frequency. To trigger externally, select either **ECL** or **TTL**, whichever applies, and connect the trigger source to the trigger **IN** input connector.

The delay between the trigger and the sample is set using the **DELAY** controls. Since the intrinsic delay is fairly substantial compared to the shorter delay ranges, it is a good idea to monitor the signal at the **GATE MON** connector and the input signal to ascertain the precise gate position.

Each time the 4121B is triggered, it ignores subsequent triggers until all actions initiated by the previous trigger have been completed. The rear-panel

BUSY OUT (TTL) signal marks the interval over which triggers are ignored. This open-collector output goes to TTL logic 0 as soon as the 4121B is triggered. When the cycle thus initiated is complete, **BUSY OUT (TTL)** goes to logic 1, indicating that the 4121B can be triggered again.

2.6.08 Busy Out vs. Sample Valid

Transitions in these two outputs define two different points in the cycle that follows each trigger. When the 4121B is triggered, both **BUSY OUT (TTL)** and **SAMPLE VALID (TTL)** go to logic 0. Following the appropriate delay, the sample is taken. At some point after that, the **AVG** and **LSO** outputs settle, that is, they become valid, and **SAMPLE VALID (TTL)** then goes positive. This positive-going transition can be used by equipment following the 4121B as a marker indicating that it is permissible to process the 4121B outputs.

Assertion of **SAMPLE VALID (TTL)** , however, does not mark the end of the cycle. The sampler circuits are automatically reset at the end of every cycle and this takes some additional time. When the reset has been accomplished, **BUSY OUT (TTL)** goes to logic 1, indicating that all activity has ended and that the 4121B can be triggered again. Hence this output becomes important in an experiment where the highest possible trigger rate must be maintained.

Model 4161A
Dual Channel ADC & Display Module

Chapter 3

3.1 Introduction

The model 4161A two channel analog-to-digital converter is used to provide display and computer interface capabilities in 4100 boxcar systems. It has two independent channels, each with its own signal and trigger inputs, and so can read and digitize the outputs of two model 4121B boxcar averager modules. In computer controlled systems, the digitized readings are transferred to the computer via the GPIB or RS232 interfaces, while in manual use they are available on the front-panel 3½ digit LED display. A separate edge-indicating analog meter is also provided which is convenient during system setup.

3.2 Installation

3.2.01 Inspection

Upon receipt the model 4161A Dual Channel ADC should be inspected for shipping damage. If any is noted, ***SIGNAL RECOVERY*** should be notified immediately and a claim filed with the carrier. The shipping container should be saved for inspection by the carrier.

3.2.02 NIM BIN Requirements

The model 4161A Dual Channel ADC is a standard double-width Nuclear Instrument Module (NIM). It requires a bin that fully conforms to the NIM standard. ***SIGNAL RECOVERY*** offer various bin options, but perhaps the most commonly used one for assembling model 4100 systems is the 4001A/4002D combination of bin and power supply. This bin allows up to four 4121B boxcar averager and two 4161A dual channel ADC modules to be accommodated and powered.

3.2.03 Grounding

The 4161A's chassis is internally returned to the third wire or grounding pin of the bin's input power connector. For equipment and operator safety, it is important that this grounding pin be returned to a good earth-ground connection via the ground wire of the power distribution system. This precaution serves to prevent shock hazards.

3.2.04 Ventilation

A standard NIM bin does not have forced air ventilation, and the model 4161A has no special ventilation requirements.

3.3 Front Panel

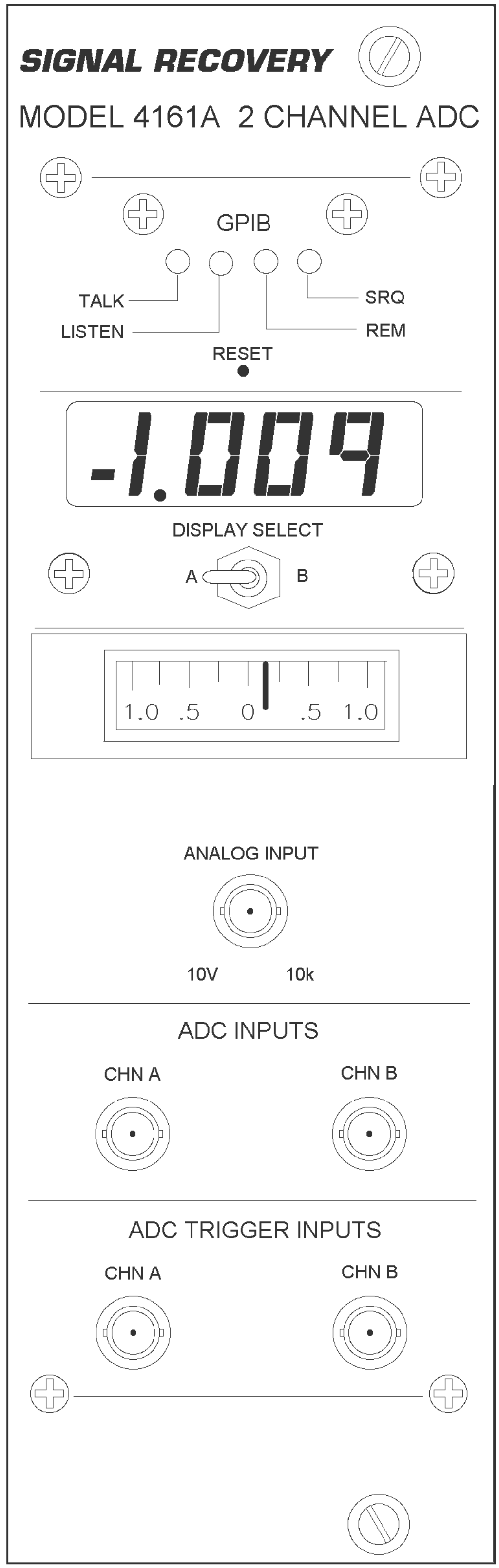

Figure 3-1, Model 4161A Front Panel

As will be seen from figure 3-1, there are four LED communications status indicators, a 3½ digit LED display and display selector toggle switch, an edge-indicating panel meter and five BNC connectors on the model 4161A front panel. The purpose of each of these items is discussed in the following sections.

3.3.01 GPIB Communications Indicators

The four LEDs located at the top of the panel have the following significance

TALK
This LED indicates that the 4161A has data ready to send to the host computer. It does not extinguish until it has finished sending this output. Note that it is not a signal that the host computer has transmitted the GPIB TALK message.

LISTEN
The listen LED lights when the first character of a command has been detected. It also operates when the unit is being controlled via the RS232 interface. It does not extinguish until the terminator is sensed. Note that this is not a signal that the host computer has transmitted the GPIB LISTEN message.

SRQ
This LED is not used with the present revision of 4161A firmware.

REM
Indicates that GPIB REM line has been asserted and the listen address applied. It does not indicate that the front panel is locked out, nor does it indicate a change in the communications receptiveness of the system. The front panel and both interfaces are always active.

3.3.02 Digital Display

The 3½ digit display can show the voltage at the **CHN A** or **CH B** inputs as selected by the associated **DISPLAY SELECT** toggle switch. The left-most digit is either unlighted or displays a "1" or "-1". The other three digits can take values of 0 through 9. Full scale display is 1.023 or -1.024, according to the input signal polarity, representing 10.23 V or -10.24 V respectively. The decimal point is fixed and always lighted.

Note that the display is only updated if the corresponding input channel is being triggered, which will only happen if there is a valid trigger signal present at the relevant **ADC TRIGGER INPUT** connector.

3.3.03 Display Select Switch

This toggle switch, located directly beneath the Digital Display, selects which of the two channels, A or B, is displayed.

3.3.04 Analog Meter

This meter is completely independent of the A/D converter functions. It monitors the voltage applied to the associated **ANALOG INPUT** BNC connector, which has an input impedance of 10 kΩ. Later units have the display marked **DC MILLIAMPERES** but an internal resistor translates the actual full-scale sensitivity to ±10 V.

3.3.05 ADC Inputs

There are two ADC inputs, one for Channel A marked **CHN A** and the other for Channel B marked **CHN B**. The analog signals to be digitized should be applied to these connectors. The input range is +10.23 V to -10.24 V DC.

3.3.06 ADC Trigger Inputs

There are two trigger inputs, one for Channel A marked **CHN A** and the other for Channel B marked **CHN B**. Each time a TTL rising-edge trigger is applied, an A/D conversion of the voltage applied to the corresponding **ADC INPUT** is initiated. The 4161A conversion time is approximately 100 µs. However, in a real computer-controlled experiment, this figure has little relevance, the limiting factor being the maximum speed at which the computer can take readings over the computer interfaces.

When the 4161A is being operated via the GPIB interface, the maximum transfer rate is typically about 150 readings per second. When using the RS232 interface at 19200 baud then the maximum rate is somewhat lower, at about 30 readings per second.

CAUTION: Because of the trigger overhead requirements, as the trigger rate is increased, less time remains to handle the data transfer. The result is a progressive decrease in the data transfer rate as the trigger rate is increased beyond a certain point. Do not attempt to maximize the data transfer rate by applying triggers at a much higher rate than the 4161A can handle.

3.3.07 Reset

A pushbutton switch is accessible through a small hole in the front panel just below the GPIB status indicators. Pressing this pushbutton resets the 4161A logic, including the A/D converters. An opened paper-clip makes a suitable tool for actuating this switch, but in normal use there should be no need to operate it.

3.4 Rear Panel

The rear panel of the 4161A, shown in figure 3-2, accommodates the two computer-interface connectors, as well as three BNC sockets and the NIM standard power socket.

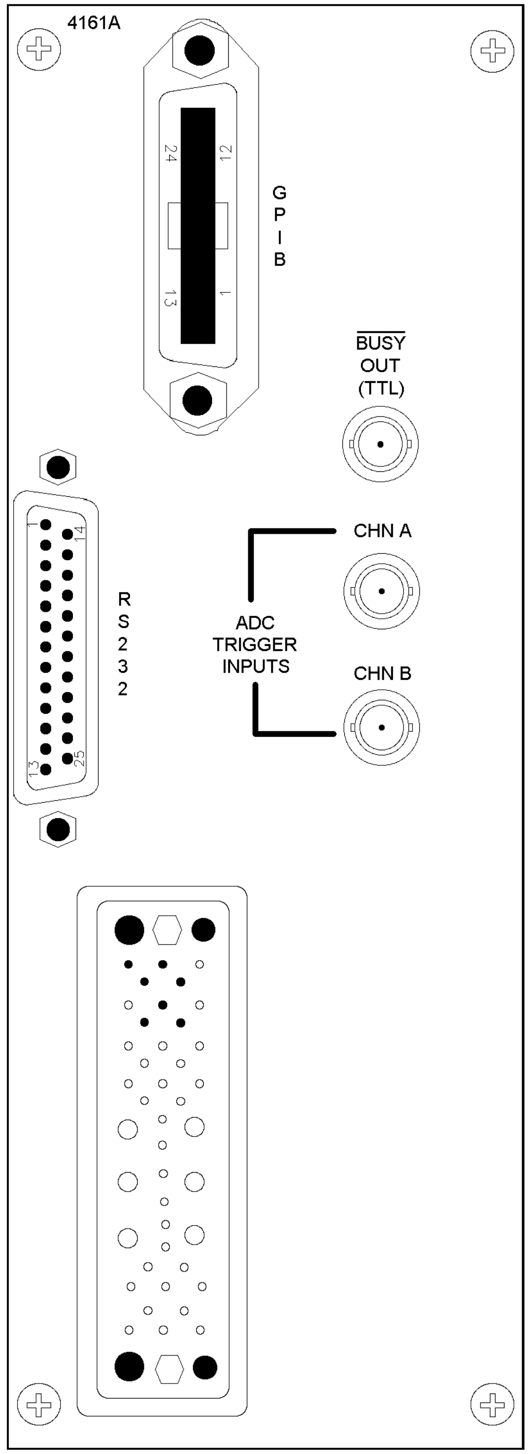

Figure 3-2, Model 4161A Rear Panel

3.4.01 RS232 Connector

This connector allows the model 4161A to be controlled via the RS232 serial interface. The 4161A is configured as a DTE (Data Terminal Equipment) and hence if it is to be connected to the standard serial port on a PC then a null modem cable will be required. The connector is shown in figure 3-3.

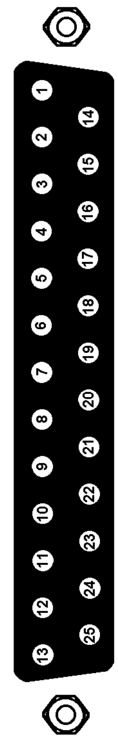

Figure 3-3, RS232 Connector (Female)

The pin allocations are as follows:-

Pin	Function	Description
1	Earth Ground	Connects the chassis of the model 4161A to that of the computer
2	Transmit Data	The 4161A transmits data on this line
3	Receive Data	The 4161A receives data on this line
4	Request to Send	This line is permanently asserted by the model 4161A, that is, it is always at a positive logic level (+10 V). As a result, the computer continuously receives the message that the model 4161A is ready to receive a command.
5	Clear to Send	The computer can control the model 4161A via this line. To enable the model 4161A to transmit, the line is placed at the positive logic level (+3 V to +12 V). To hold off transmission by the model 4161A, the line must be at the negative logic level (-3 V to -12 V). Once this line goes positive, data transfer, if initiated by an appropriate command, will proceed rapidly. This line is returned to +12 V via an internal resistor so that, if left unconnected,

		the 4161A is allowed unimpeded transmission.
7	Logic Ground	Data signal levels should be with reference to logic ground. The logic ground line of the model 4161A should interconnect with the logic ground line of the computer.

All other pins are not connected.

Diagrams of cables suitable for connecting this port to the RS232 port of PC computers are shown in figures 3-4 and 3-5. Users with reasonable practical skills can easily assemble these cables from parts which are widely available through computer stores and electronics components suppliers.

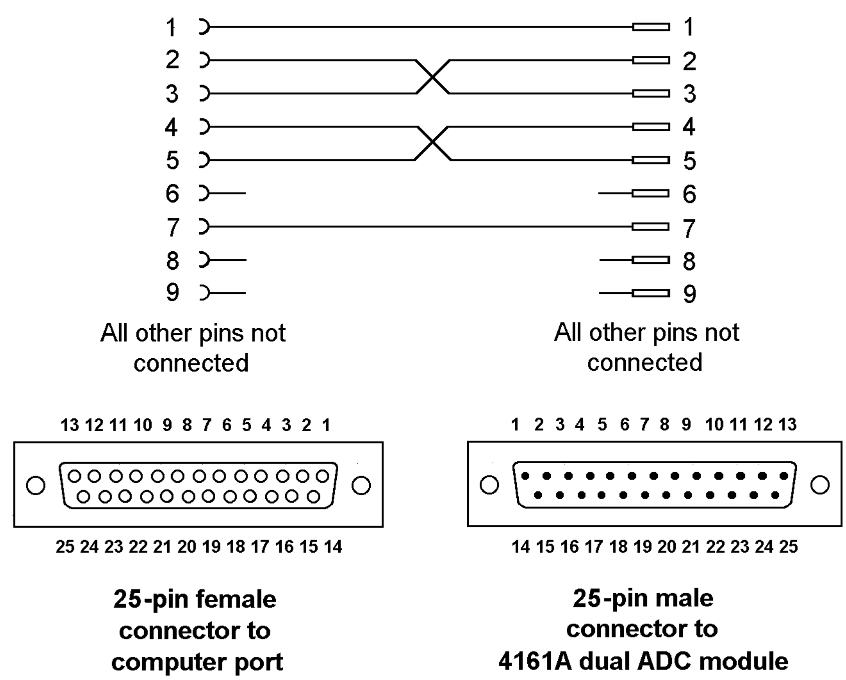

Figure 3-4, Interconnecting RS232 Cable Wiring Diagram

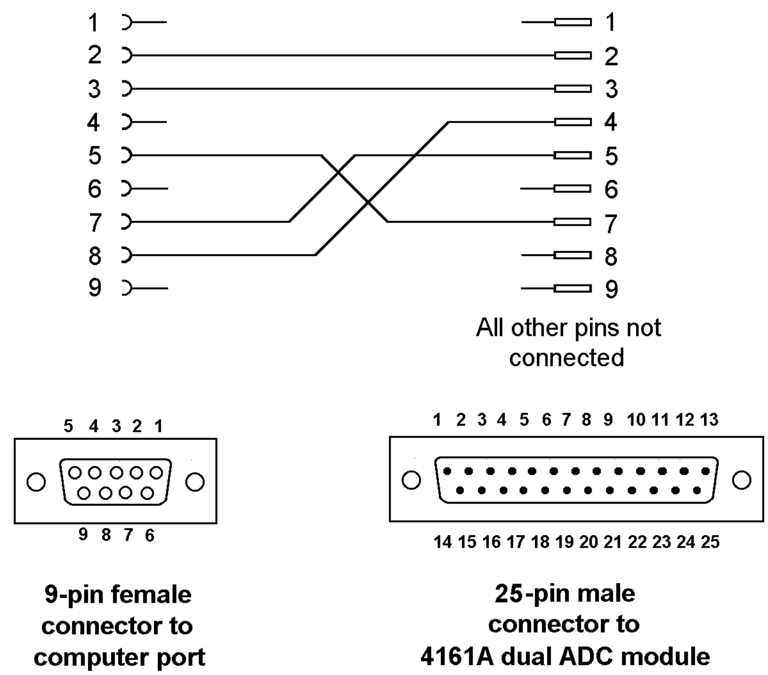

Figure 3-5, Interconnecting RS232 Cable Wiring Diagram

3.4.02 GPIB Connector

This connector allows the model 4161A to be controlled via the GPIB (IEEE-488) parallel interface. It requires that a GPIB cable be connected from the computer's IEEE-488 GPIB port to this connector. The connector pin allocation complies fully with the GPIB standard.

3.4.03 BUSY OUT (TTL)

This open-collector TTL output is used to allow the controlling computer to regulate the rate of data acquisition of a 4100 boxcar averager system, by holding off triggers to the system until the 4161A ADC module is able to accept and process them.

Under computer control, the **BUSY OUT (TTL)** operates as follows:-

1) Remains at logic 0 until an appropriate command is issued by the computer

2) Goes to logic 1, releasing external trigger hold-off circuitry (such as can be provided by the ***SIGNAL RECOVERY*** model 9650A digital delay generator)

3) Returns to logic 0 on receipt of a trigger signal at either the **CHN A** or **CHN B** ADC trigger inputs, and remains there while each measured value is transferred back to the computer and thereafter until the next synchronized read command.

3.4.04 ADC TRIGGER INPUTS

These two connectors duplicate the connectors of the same name mounted on the front panel (see section 3.3.06).

CAUTION: Do not connect ADC trigger signals to both the front and rear-panel CHN A or CHN B ADC trigger input connectors. Use only one trigger input signal for each ADC.

3.4.05 NIM Power Connector

The power and ground connections are made via this connector, as follows.

Pin	Function
11	-6 V
17	-12 V
28	+24 V
29	-24 V
34	GROUND
16	+12 V
10	+6 V

3.5 Operation

3.5.01 Introduction

Operation of the model 4161A is extremely simple. Each time a trigger is applied to either of the two channels, the voltage at the corresponding ADC Signal Input connector undergoes an analog-to-digital conversion. The resulting number is latched so that it can be conveniently read by the host computer via the RS232 or GPIB interfaces.

With respect to the front panel, other than to connect the cables as previously described, there are no operator considerations other than the option of displaying the voltage of either input channel on the front panel LED display, using the **DISPLAY SELECT** switch to choose A or B.

When using the model 4161A to implement a computer controlled system, the GPIB interface is the more reliable and faster option, so if there is the choice of using GPIB or RS232 interfacing the former method is to be preferred.

3.5.02 GPIB Interface Configuration

The GPIB communications settings are adjusted using a DIP switch on the 4161A's main PCB assembly. To check, and if necessary change, these settings proceed as follows.

1) Turn off the power to the NIM rack and remove the model 4161A.

2) Place the model 4161A on a flat surface so that the front panel of the module is to

the right and the bottom edge closest to you.

3) Remove the four Posidriv screws holding the cover in place.

4) Locate the communications DIP switches, positioned just below the vertical center line of the board and about centrally horizontally. These switches are shown in figure 3-6

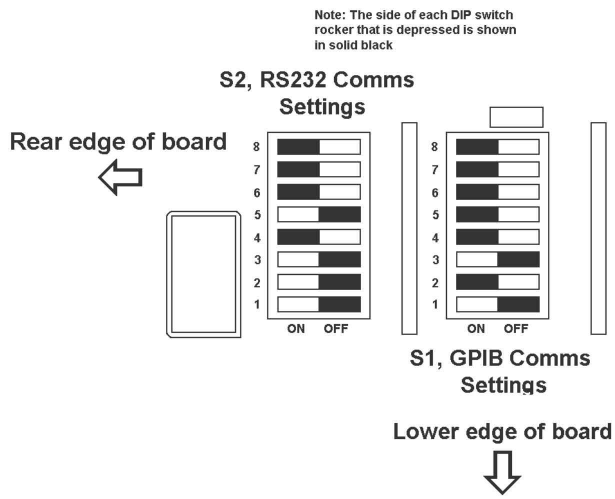

Figure 3-6, Model 4161A Communications Settings DIP Switches

Switch pack S1, the right-hand one of the pair, sets the GPIB communications parameters. The function of each element of this switch is shown in figure 3-7.

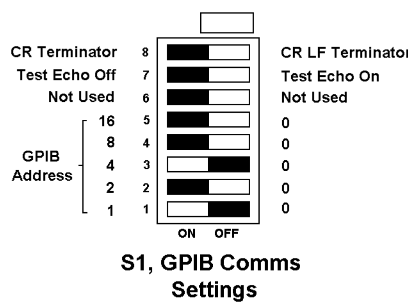

Figure 3-7, Model 4161A GPIB Communications Settings DIP Switch

5) Set the GPIB address by setting the switches S1-1 to S1-5 according to the following table:

GPIB Address	S1-1	S1-2	S1-3	S1-4	S1-5
1	OFF	ON	ON	ON	ON
2	ON	OFF	ON	ON	ON
3	OFF	OFF	ON	ON	ON
4	ON	ON	OFF	ON	ON
5	OFF	ON	OFF	ON	ON
6	ON	OFF	OFF	ON	ON
7	OFF	OFF	OFF	ON	ON
8	ON	ON	ON	OFF	ON
9	OFF	ON	ON	OFF	ON
10	ON	OFF	ON	OFF	ON
11	OFF	OFF	ON	OFF	ON
12	ON	ON	OFF	OFF	ON
13	OFF	ON	OFF	OFF	ON
14	ON	OFF	OFF	OFF	ON
15	OFF	OFF	OFF	OFF	ON
16	ON	ON	ON	ON	OFF
17	OFF	ON	ON	ON	OFF
18	ON	OFF	ON	ON	OFF
19	OFF	OFF	ON	ON	OFF
20	ON	ON	OFF	ON	OFF
21	OFF	ON	OFF	ON	OFF
22	ON	OFF	OFF	ON	OFF
23	OFF	OFF	OFF	ON	OFF
24	ON	ON	ON	OFF	OFF
25	OFF	ON	ON	OFF	OFF
26	ON	OFF	ON	OFF	OFF
27	OFF	OFF	ON	OFF	OFF
28	ON	ON	OFF	OFF	OFF
29	OFF	ON	OFF	OFF	OFF
30	ON	OFF	OFF	OFF	OFF
31	OFF	OFF	OFF	OFF	OFF

Table 3-1, GPIB Address Selection

Note that a switch is ON when the left-hand edge of the relevant rocker is depressed. As an example, in the diagram shown in figure 3-7 the GPIB address is set to the factory default value of “5”.

6) Set the terminator as required. In GPIB communications the model 4161A accepts either <CR> or <CR><LF> or the GPIB line EOI sent with the last byte as a command terminator for commands it receives. It always appends a terminator to the transmitted data value, either <CR> or <CR><LF>, as set by Switch 8 of the GPIB switch S1 (see figure 3-7). In addition it asserts the GPIB line EOI with the last byte of the transmission. The selected terminator must be acceptable to the host computer. It is not always easy to check reference documentation to determine a computer's terminator requirement. Where this is the case, one can simply try first one possibility and then the other. One will work.

NOTE: The terminator selection affects both RS232 and GPIB interfaces.

7) Set the Test Echo switch as required. When the Test Echo mode is turned on, the 4161A echoes every character received at the GPIB interface to the RS232 interface, which can be useful for diagnostic purposes during program debugging.

   NOTE: In normal use the test echo function should be turned off.

8) Once the GPIB settings match those required, replace the module cover removed earlier in this procedure and secure using the four Posidriv screws.

This completes the procedure for configuring the GPIB interface.

3.5.03 GPIB Interface Operation

Except for the two specialized commands, X and Y described later in section 3.5.06, when using the GPIB interface the controlling program should use the GPIB serial poll status byte. This contains information which must be urgently conveyed from the instrument to the controller.

The function of the individual bits in the status byte is instrument dependent, apart from bit 6 (the request service bit) whose function is defined by the standard. The allocations in the case of the 4161A are give in table 3-2.

Bit	Function	Comment
Bit 0 (LSB)	Command Complete	Bit 0 is cleared when the model 4161A is busy executing a command. It is set when execution of the previous command is complete.
Bit 1	Command Error	Bit 1 is set when a command error occurs. It is cleared when the next valid command is issued.
Bit 2	Not Used	
Bit 3	Not Used	
Bit 4	A/D of A done	RDA command can be applied.
Bit 5	A/D of B done	RDB command can be applied.
Bit 6	Service Request	Not used in model 4161A
Bit 7 (MSB)	Data Available	Bit 7 is set when the model 4161A has output ready to transfer to the computer. It is cleared when the 4161A has no output waiting.

Table 3-2, Model 4161A Serial Poll Status Byte

As can be seen, bits 0 and 7 signify "command complete" and "data available" respectively. In GPIB communications, the use of these bits can lead to a useful simplification of the control program by providing a response subroutine which is the same for all commands, whether or not they send a response over the bus. The subroutine should carry out the following sequence of events:

1) Send the command

2) Perform repeated serial poll operations in a loop until bit 0 (command complete) is zero. This implies that the command has been received by the instrument and is being processed. However, it is possible that if the command were a write-only command and a slow computer were being used then the instrument may actually clear and then reset bit 0 (i.e. actually complete the command) before the first serial poll operation were executed. Hence the loop must include the provision to timeout under these conditions; a value of 10 ms should be satisfactory in most cases.

3) If bit 0 clears, perform repeated serial polls testing both bit 0 and bit 7 (data available) and, if bit 7 is asserted then perform a read operation. This cycle (i.e. test bit 0 (command complete) and test bit 7 (data available)) should then continue until the 4161A asserts bit 0 to indicate that the command-response sequence is complete, so that it is ready for the next command.

This procedure, although apparently complex, deals successfully with all commands.

3.5.04 RS232 Interface Configuration

As with the GPIB interface, the RS232 communications settings are adjusted using a DIP switch on the 4161A's main PCB assembly. To check, and if necessary change, these settings proceed as follows.

1) Turn off the power to the NIM rack and remove the model 4161A.

2) Place the model 4161A on a flat surface so that the front panel of the module is to the right and the bottom edge closest to you.

3) Remove the four Posidriv screws holding the cover in place.

4) Locate the communications DIP switches, positioned just below the vertical center of the board and about centrally horizontally. These switches are shown in figure 3-6 above. Switch pack S2, the left-hand of the pair, sets the RS232 communications parameters. The function of each switch element is shown in figure 3-8.

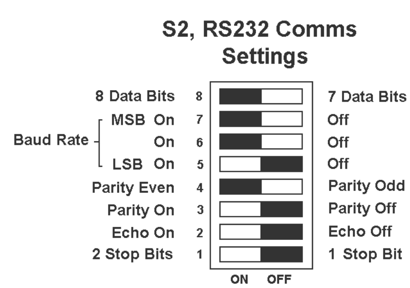

Figure 3-8, Model 4161A RS232 Communications Settings DIP Switch

5) Set the number of data bits to 7 or 8 using the switch S2-8.

6) Set the RS232 baud rate by adjusting switches S2-5, S2-6 and S2-7 according to the diagram shown in figure 2-9.

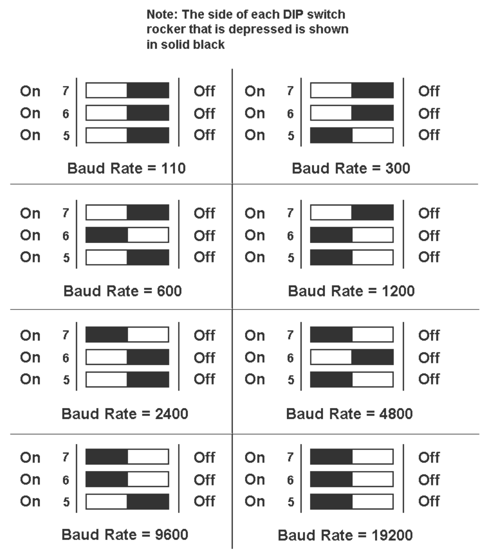

Figure 3-9, Model 4161A RS232 Baud Rate Settings using Switch S2

As an example, in the diagram shown in figure 3-8 the baud rate is set to the factory default value of 9600 baud.

6) Set the parity to even or odd and turn it on or off as required using the switches S2-4 and S2-3.

7) Switch S2-2 turns the RS232 character echo mode on or off. When the echo mode is turned on, every character received at the RS232 interface is echoed back to it. This provides a convenient way of performing a “software handshake” preventing command overruns. The principle is that the controlling program sends a command one character at a time, waiting until the 4161A has echoed each character before sending the next one.

NOTE: Do not confuse the RS232 Echo Mode with the GPIB Test Echo Mode.

8) Set the number of stop bits to 1 or 2 using the switch S1-1

9) Refer to figure 2-7 and locate the GPIB communications settings switch S1. The termination option is common to both GPIB and RS232 interfaces and hence is set by switch S1-8. The model 4161A accepts either <CR> or <CR><LF> as command terminator for commands it receives on the RS232 interface. In turn, the terminator it appends to a transmitted data value, either <CR> or <CR><LF>, is set by switch S1-8. The selected terminator must be acceptable to the host computer. It is not always easy to check reference documentation to determine a computer's terminator requirement. Where this is the case, one can simply try both settings to identify the correct one.

NOTE: The terminator selection affects both RS232 and GPIB interfaces.

10) Once the RS232 settings match those required, replace the module cover removed earlier in this procedure and secure using the four Posidriv screws.

This completes the procedure for configuring the RS232 interface.

3.5.05 RS232 Interface Operation

The 4161A supports three different methods of handshaking, which ensure that individual characters of an RS232 transmission to it or generated by it do not overrun.

Hardware Handshaking using Clear-to-Send
If Clear-to-Send control is selected, the RS232 line clear-to-send (CTS) must be asserted before the 4161A will transmit data. (If CTS is left unconnected, it will float to the "asserted" state.) The data stream can be cut off by making CTS negative. Making CTS positive restores the data flow.

If CTS is made negative, the model 4161A will finish transmitting the character being processed at that moment, and may transmit one or two additional characters as well. The computer's software must be able to anticipate and handle the additional characters.

Note that CTS is returned to +12 V through a pull-up resistor inside the model 4161A so that it is allowed unimpeded transmission if the line is left floating.

When setting up CTS control, the pin connections will depend on whether the computer's RS232C interface is configured as a DTE or DCE device. Request-to-Send (RTS) and CTS are complementary handshake lines. In a DTE device, such as the model 4161A, CTS is an input and RTS an output. Therefore, if the computer's interface is also a DTE device the RTS and CTS connections must be cross-wired in order to get satisfactory operation.

Software Handshaking using XON/XOFF Control
If XON/XOFF control is selected, the "characters" XOFF (Control-S or ASCII decimal 19) and XON (Control Q or ASCII decimal 17) are used to control RS232C data transmission. Sending XOFF will prevent RS232C transmissions. If applied during a transmission, the transmission will halt. However, the host computer must be ready to accept a couple more characters after it transmits XOFF. XOFF does not prevent characters from being echoed if the ECHO mode is ON. Transmission resumes when XON (Control Q) is applied.

Software Handshaking using Character Echo
When the character echo mode is turned on using switch S2-2 (figure 3-8), every character received at the 4161A’s RS232 interface is echoed back to it. This provides a convenient way of performing a “software handshake” preventing command overruns. The principle is that the controlling program sends a command one character at a time, waiting until the 4161A has echoed each character before sending the next one.

NOTE: With modern computers the rate at which the 4161A sends characters over the RS232 interface is rarely a problem. The limiting factor is often the rate at which it can accept them. Hence it is recommended that only the character echo handshake for transmissions to the 4161A be used.

When using the RS232 interface, it is important to ensure that a new command is not sent before the model 4161A has finished processing the previous command. In order to facilitate this, therefore, the 4161A sends a character at the same time as bit 0 becomes asserted in the status byte when using GPIB communications. This character is sent out by the 4161A after each command response (whether or not the response includes a transmission over the interface) to indicate that the response is finished and that it is ready for a new command. The prompt takes one of two forms. If the command contained an error, either in syntax or by a command parameter being out of range the prompt is ? (ASCII 63). Otherwise the prompt is * (ASCII 42).

The error condition corresponds to the assertion of bit 1 (command parameter error) in the GPIB status byte.

The prompts are a rapid way of checking on the instrument status and enable a convenient keyboard control system to be set up simply by attaching a standard terminal, or a simple computer-based terminal emulator, to the RS232 port.

3.5.06 Commands

The model 4161A responds to a range of ASCII commands which are used to control the method by which it digitizes applied voltages and to return the measured values. A valid transmission to the to the 4161A consists of one of these commands followed by a terminator, either Carriage Return <CR> or Carriage Return Followed by a Line Feed <CR><LF>. All but two of the commands can be applied via either the GPIB or RS232C interface, both of which are always active, with the other two being suitable only for the GPIB interface. The format and function of each command is as follows.

NOTE: All commands use upper-case ASCII characters.

ID Identification

Causes the 4161A to respond with the number 4161.

BIN 1 Set response mode to binary

This command activates the binary transfer mode, in which the responses to the RDA, RDB, SA, & SB commands are of the following format:

<low_byte><high_byte>

When using GPIB transmission, the GPIB EOI line is asserted on the second byte. The upper four bits of the high byte are always zero; the overall full-scale range of the 12 bytes that are left is ±2048. Somewhat higher data transfer rates can be achieved in the binary response mode than in the ASCII response mode.

Similarly, the response format for the RAB and SAB commands becomes:

<low_byte_A><high_byte_A><low_byte_B><high_byte_B>

EOI is asserted on the fourth byte.

BIN 0 Set response mode to ASCII
This command activates the default (power-up) ASCII transfer mode, in which the responses to the RDA, RDB, SA, & SB commands are ASCII strings of the following format:

<digit><digit><digit><space><CR>
(e.g., "255 <CR>")

Similarly, the response format for the RAB and SAB commands becomes:

<digit><digit><space>,<digit><digit><space><CR>
(e.g., "34 ,82 <CR>")

When using GPIB transmission, EOI is asserted on the last byte.

RDA Read voltage at **CHN A** Input
Reads the voltage at the **CHN A** input connector as sampled by the most recent trigger at the **CHN A** ADC trigger input connector and returns the value. The number returned is the number of A/D counts, and is double the number displayed on at the front panel. With a ±F.S. input applied, the response is 2047 or -2048, i.e. each count is 5 mV.

Note that RDA is a non-synchronous read command, that is, it has no effect on the 4161A's rear-panel **BUSY OUT (TTL)** output.

RDB Read voltage at **CHN B** Input
Reads the voltage at the **CHN B** input connector as sampled by the most recent trigger at the **CHN B** ADC trigger input connector and returns the value. The number returned is the number of A/D counts, and is double the number displayed on at the front panel. With a ±F.S. input applied, the response is 2047 or -2048, i.e. each count is 5 mV.

Note that RDB is a non-synchronous read command, that is, it has no effect on the 4161A's rear-panel **BUSY OUT (TTL)** output.

RAB Read voltages at **CHN A** and **CHN B** Inputs
This command is equivalent to sending RDA followed by RDB.

As with RDA and RDB, this command is non-synchronous.

Synchronized Operation

In some experiments the previously described commands are not suitable for acquiring and transferring data rapidly. The problem is that the system can be triggered before transfer of the result of the previous A/D conversion is complete, causing synchronization to be loss. The commands described in the following paragraphs remedy this problem by using the 4161A's **BUSY OUT (TTL)** output to control the trigger receptiveness of the system in such a way as to keep the transfer of data to the host computer synchronized. When using these commands there is one A/D conversion and one data transfer to the computer for each trigger accepted by the system.

In order to use this technique the **BUSY OUT (TTL)** output must be cabled to both the **BUSY OUT (TTL)** output of all of the 4121B boxcar averagers used in the system and to the source of system trigger in such a way that when the **BUSY OUT (TTL)** line is low triggers are inhibited. If the system uses a ***SIGNAL RECOVERY*** model 9650A digital delay generator then this can be achieved by connecting the **BUSY OUT (TTL)** line to that unit's **ABORT INH** input, but in other systems then the same effect should be obtained using other suitable methods.

BSYON Activate **BUSY OUT (TTL)** control.

This command causes the **BUSY OUT (TTL)** output to go low, inhibiting system triggers. It remains low unless:

1) BSYOFF is applied, restoring non-synchronized **BUSY OUT (TTL)** control, or:

2) One of the synchronized-mode read commands, SA, SB, or SAB is applied. Each time one of these commands is received, **BUSY OUT (TTL)** goes high, allowing the system to receive a trigger. The boxcar averager takes a sample and in turn triggers the relevant channel of the 4161A. **BUSY OUT (TTL)** immediately goes low, preventing another trigger, allowing the 4161A as much time as it needs to complete the conversion and for the resulting value to be transferred to the computer.

   NOTE: In normal non-synchronized operation, the 4161A holds BUSY OUT (TTL) low only from the arrival of the A/D Trigger to completion of the A/D conversion. BUSY OUT (TTL) is not held low during data transfer to the computer.

BSYOFF Deactivates **BUSY OUT (TTL)** control.

SSF Initializes the 4161A for synchronous-mode operation

The SSF command must be applied after the BSYON command to establish synchronous operation. Once it has been applied, any number of SA, SB, or SAB commands may be used to read the data during the experiment.

CSF Resets the 4161A to asynchronous-mode operation

This command tells the 4161A to exit the synchronous mode. It is normally applied after the last SA, SB, or SAB command and before the BSYOFF command.

SA Synchronously read voltage at **CHN A** input

Releases **BUSY OUT (TTL)** to allow a system trigger to be occur. On receipt of a trigger at the **CHN A** ADC trigger input connector, which then samples and digitizes the voltage at the **CHN A** input connector, the **BUSY OUT (TTL)** line is pulled low, preventing further triggers. The number returned is the number of A/D counts, and is double the number displayed on at the front panel. With a ±F.S. input applied, the response is 2047 or -2048, i.e. each count is 5 mV.

SB Synchronously read voltage at **CHN B** input
Releases **BUSY OUT (TTL)** to allow a system trigger to be occur. On receipt of a trigger at the **CHN B** ADC trigger input connector, which then samples and digitizes the voltage at the **CHN B** input connector, the **BUSY OUT (TTL)** line is pulled low, preventing further triggers. The number returned is the number of A/D counts, and is double the number displayed on at the front panel. With a ±F.S. input applied, the response is 2047 or -2048, i.e. each count is 5 mV.

SAB Synchronously read voltages at **CHN A** and **CHN B** inputs
Releases **BUSY OUT (TTL)** to allow a system trigger to be occur. On receipt of triggers at *both* the **CHN A** and **CHN B** ADC trigger input connectors, which also sample the corresponding voltages at the **CHN A** and **CHN B** input connectors, the **BUSY OUT (TTL)** line is pulled low, preventing further triggers. The response is of the same format as the RAB command.

DSPON Turn display lights on.
This command turns on the front panel LEDs and 7-segment indicators.

DSPOFF Turn display lights off.
This command turns off the front panel LEDs and 7-segment indicators.

Binary Data Transfer Mode Operation - GPIB Interface Only

X Initiates the binary data transfer mode for Channel A
This mode allows the system to take data and transfer it to the computer as rapidly as possible. Applying the command once activates the mode and pulls the **BUSY OUT (TTL)** output low. On receipt of a GPIB read command the 4161A releases the **BUSY OUT (TTL)** to allow a system trigger to occur. Once a trigger has been received at the **CHN A** trigger input connector, the voltage at the **CHN A** input connector is sampled and digitized, and the **BUSY OUT (TTL)** is again pulled low, preventing further triggers.

The digitized voltage is transferred as two eight-bit binary bytes, with the high-order byte transferred first. The data, eleven bits plus sign, occupies all of the high-order byte and the four highest bits of the low-order byte. The host computer has to do an unsigned shift of the data four places to the right to remove the four low bits of the low-order byte. With a positive full-scale input applied, the transferred number (after removing the four low bits of the low-order byte) is 111111111111. With a negative full-scale input applied, the transferred number (after removing the four low bits of the low-order byte) is 000000000000. The decimal equivalents of these two values are +4096 and 0. Thus, to convert to a bipolar representation, the computer must subtract 2048 from the decimal equivalent of the transferred value.

The mode is terminated by sending any other valid command except the Y command.

Y Initiates the binary data transfer mode for Channel B
This mode allows the system to take data and transfer it to the computer as rapidly as possible. Applying the command once activates the mode and pulls the **BUSY OUT (TTL)** output low. On receipt of a GPIB read command the 4161A releases the **BUSY OUT (TTL)** to allow a system trigger to occur. Once a trigger has been received at the **CHN B** trigger input connector, the voltage at the **CHN B** input connector is sampled and digitized, and the **BUSY OUT (TTL)** is again pulled low, preventing further triggers.

The digitized voltage is transferred as two eight-bit binary bytes, with the high-order byte transferred first. The data, eleven bits plus sign, occupies all of the high-order byte and the four highest bits of the low-order byte. The host computer has to do an unsigned shift of the data four places to the right to remove the four low bits of the low-order byte. With a positive full-scale input applied, the transferred number (after removing the four low bits of the low-order byte) is 111111111111. With a negative full-scale input applied, the transferred number (after removing the four low bits of the low-order byte) is 000000000000. The decimal equivalents of these two values are +4096 and 0. Thus, to convert to a bipolar representation, the computer must subtract 2048 from the decimal equivalent of the transferred value.

The mode is terminated by sending any other valid command except the X command.

NOTE: No terminators, other than the GPIB EOI line, are sent in the binary-transfer mode. Also, to get the fastest possible transfer rate, the front-panel display and LED's are turned off in the binary transfer mode, which might cause the user to inadvertently infer that the 4161A has lost power.

3.6 Sample Programs

3.6.01 Introduction

This section gives some examples of the commands that need to be sent to the 4161A in typical experimental situations.

3.6.02 Simple Dual Channel ADC

In this case the signals to be digitized are connected to the **CHN A** and/or **CHN B** ADC inputs, with corresponding trigger signals to the **CHN A** and/or **CHN B** ADC trigger inputs. The commands to read these values are then simply:-

RDA	Reads **CHN A** input voltage
RDB	Reads **CHN B** input voltage
RAB	Reads **CHN A** and **CHN B** input voltages

3.6.03 Dual Channel ADC with System Trigger Holdoff

In this case the synchronized read mode of operation is used. In order to use this technique the **BUSY OUT (TTL)** output must be cabled to both the **BUSY OUT (TTL)** output of all of the 4121B boxcar averagers used in the system and to the source of system trigger in such a way that when the **BUSY OUT (TTL)** line is low triggers are inhibited. If the system uses a ***SIGNAL RECOVERY*** model 9650A digital delay generator then this can be achieved by connecting the **BUSY OUT (TTL)** line to that unit's **ABORT INH** input, but in other systems then the same effect should be obtained using other suitable methods.

The signals to be digitized are connected to the **CHN A** and/or **CHN B** ADC inputs, with corresponding trigger signals to the **CHN A** and/or **CHN B** ADC trigger inputs.

The commands to operate this mode are then as follows:

BSYON	Forces **BUSY OUT (TTL)** low.
SSF	Establishes synchronized mode.
begin loop	Loop for required number of data points
SA, SB or SAB	Initiate cycle which: a) Releases **BUSY OUT (TTL)** b) Waits for trigger at **CHN A** and/or **CHN B** trigger input(s). c) Pulls **BUSY OUT (TTL)** low d) Digitizes **CHN A** and/or **CHN B** ADC input value(s). e) Transfers data back
end loop	
CSF	Ends synchronized mode.
BSYOFF	Re-establishes normal **BUSY OUT (TTL)** control.

3.6.04 Single Channel ADC with Binary Transmission

This mode is suitable for GPIB use only. It requires the same connections to the **BUSY OUT (TTL)** output as described in section 3.6.03 above.

The signals to be digitized are connected to the **CHN A** and/or **CHN B** ADC inputs, with corresponding trigger signals to the **CHN A** and/or **CHN B** ADC trigger inputs.

The commands to operate this mode are then as follows:

BSYON	Forces **BUSY OUT (TTL)** low.
SSF	Establishes synchronized mode.
begin loop	Loop for required number of data points
GPIB Write "X"	Establish fast transfer mode for **CHN A**
GPIB Read 2 bytes	Initiate cycle which: a) Releases **BUSY OUT (TTL)** b) Waits for trigger at **CHN A** trigger input. c) Pulls **BUSY OUT (TTL)** low d) Digitizes **CHN A** ADC input value. e) Transfers data back
end loop	
BSYOFF	Re-establishes normal **BUSY OUT (TTL)** control.

System Configuration Guide

Chapter 4

4.1 Introduction

This chapter describes the modules required to assemble typical systems using model 4100 series components and gives the necessary interconnections. In addition to the main units you will also need a ready supply of suitable 50 Ω BNC cables, BNC "tee" pieces and BNC 50 Ω terminators. Such items, if not already to hand, are widely available from electronics component suppliers.

4.2 System Configurations

4.2.01 Single Channel Static Gate Manual System

Required Equipment:

- Model 4121B Boxcar Averager
- NIM Bin and power supply, such as model 4001A/4002D

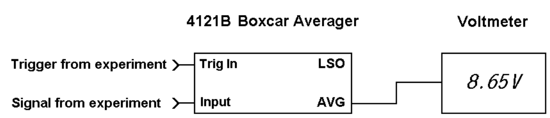

Figure 4-1, Single Channel Static Gate Manual System

The system is shown above in figure 4-1.

The 4121B is mounted in the NIM bin (not shown) and the trigger and signal from the experiment applied to it. The internal trigger delay generator is used to set the gate position at the required point on the signal waveform and the output averager controls are adjusted to give the required output stability. A voltmeter is used to monitor the measured signal.

4.2.02 Single Channel Waveform Recording System using ADC/DAC PC Card

Required Equipment:

- Model 4121B Boxcar Averager
- NIM Bin and power supply, such as model 4001A/4002D
- PC interface card offering at least one ADC input and one DAC output with ±10 V FS range, 12 bits or better (not available from ***SIGNAL RECOVERY***)

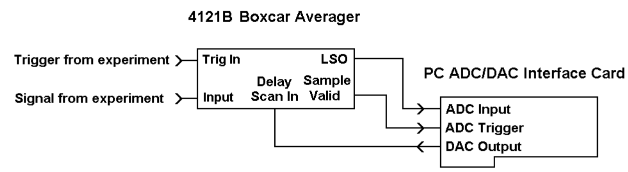

Figure 4-2, Single Channel Waveform Recording System using ADC/DAC PC Card

The system is shown above in figure 4-2.

In this case the DAC output of a third-party ADC/DAC plug-in card for a PC is used to generate a control voltage for the internal trigger delay generator of the 4121B, which is housed in the NIM bin (not shown). The 4121B's last sample output is cabled to the card's ADC input, and the sample valid output is used as an external trigger input for the card's ADC. User-developed software generates a staircase ramp waveform at the DAC output that sweeps the sampling gate across the desired delay range, and at each step acquires and digitally averages the required number of sample values. The resulting waveform record is stored to file for subsequent display and analysis.

4.2.03 Single Channel System with Baseline Subtraction

Required Equipment:

- Model 4121B Boxcar Averager
- NIM Bin and power supply, such as model 4001A/4002D
- Optical Chopper with external reference frequency input to set chopping frequency, such as the ***SIGNAL RECOVERY*** model 197 or 650 series.

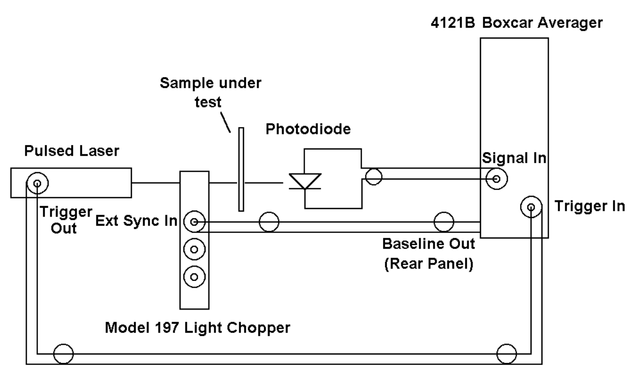

Figure 4-3, Single Channel System with Baseline Subtraction

The system is shown above in figure 4-3.

A pulsed laser running at 1 kHz is passed through a model 197 light chopper to the sample under test and thence to the photodiode detector. The 4121B, which is housed in the NIM bin (not shown), is set to the Baseline 1 sampling mode and triggered from the laser. In this mode, the **BASELINE I/O (TTL)** line on the 4121B is an output which with a 1 kHz trigger rate will be at 500 Hz. This output is connected to the model 197 light chopper's external sync input, causing the chopper to run at 500 Hz. With suitable positioning this means that alternate laser pulses do not reach the sample, so that alternate samples correspond to "signal" and "baseline" values.

The 4121B performs an automatic subtraction of these samples to give automatic baseline removal.

4.2.04 Two Channel Static Gate System with GPIB Interface

Required Equipment:
- Two Model 4121B Boxcar Averagers
- One Model 4161A Dual ADC and Display Module
- NIM Bin and power supply, such as model 4001A/4002D

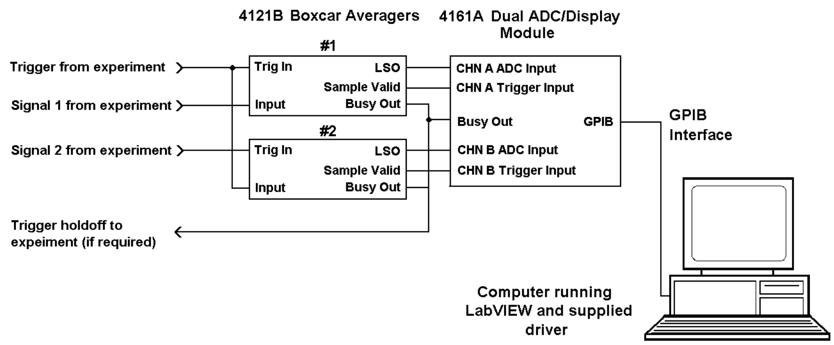

Figure 4-4, Two Channel Static Gate System with GPIB Interface

The system is shown above in figure 4-4.

One model 4161A ADC module is used to digitize the outputs generated by two model 4121B boxcar averagers, with all three units being mounted in the NIN bin (not shown). The computer controls the rate of acquisition via the 4161A. In cases of high trigger rates (typically greater than 50 - 100 Hz) the 4161A's **BUSY OUT (TTL)** output can be used to holdoff the experimental trigger to allow the computer to control the number of trigger cycles.

4.2.05 Four Channel Waveform Recording System using Model 9650A DDG

Required Equipment:
- Four Model 4121B Boxcar Averagers
- Two Model 4161A Dual ADC and Display Modules
- ***SIGNAL RECOVERY*** Model 9650A four channel digital delay generator fitted with /97 GPIB interface option
- NIM Bin and power supply, such as model 4001A/4002D

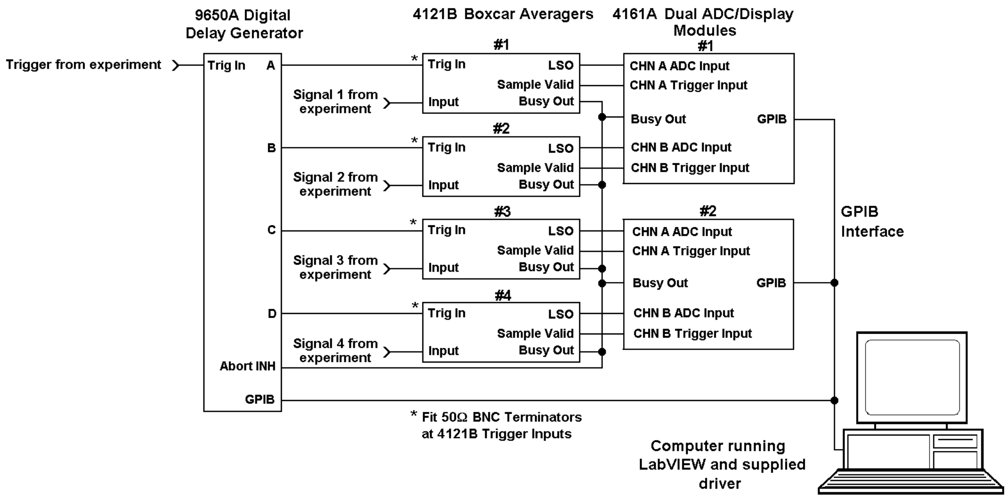

Figure 4-5, Four Channel Waveform Recording System using Model 9650A DDG

The system is shown above in figure 4-5.

Two model 4161A ADC modules are used to digitize the outputs generated by four model 4121B boxcar averagers, with all six units being mounted in the NIN bin (not shown). In addition a model 9650A four channel digital delay generator fitted with a GPIB interface is used to generate delayed triggers to each of the four boxcar averagers.

The 9650A output levels should be set to +5 V and connected to the trigger inputs of the 4121B's. In order to avoid errors due to trigger pulse reflection it is advisable to use 50 Ω terminators at the 4121B end of each trigger cable.

The computer controls the rate of acquisition via the 4161A, by means of the **BUSY OUT (TTL)** output. This is used to holdoff the trigger to the system by preventing the 9650A from triggering whenever data is still being processed from an earlier trigger.

Specifications

Appendix **A**

Model 4121B Boxcar Averager

General

Single-channel gated integrator module mounted in NIM enclosure with adjustable sensitivity, offset, gatewidth and output averager. Manual controls.

Analog gate delay generator with manual or DC voltage control.

Measurement Modes

On receipt of an external trigger, the instrument waits for the preset gate delay and then integrates the voltage present at its input for the preset gate width. On completion a DC voltage representing this integral is provided at the Last Sample Output connector and in addition fed forward into an analog integrator stage.

Signal Channel

Mode	Normal or Baseline Sampling
Sensitivity	±20 mV to ±2 V in 1-2-5 sequence
Coupling	AC/DC
Impedance	
DC only	50 Ω // 10 pF
DC or AC	1 MΩ // 30 pF
Maximum Safe Input	
50 Ω Input	±5 V
1 MΩ Input	±100 V
Offset	
20 mV - 200 mV sensitivity	±10 × FS; non-removable
500 mV - 2 V sensitivity	±2 V; non-removable
Overload Indicator	LED
Overload Level	Input (signal plus noise) > 1.1 × FS
Overload Recovery	Recovers after 1 sample for ×10 overload
Gain Drift	0.5 % /°C, gate width > 30 ns; 1.0 % /°C, gate width < 10 ns
DC Drift (referred to input)	
	0.2 %/°C, gate width > 20 ns; 1.0 %/°C, gate width < 20 ns
Bandwidth	
50 Ω input	DC to 450 MHz
1 MΩ DC input	DC to 100 MHz
1 MΩ AC input	1.5 Hz to 100 MHz
Signal Risetime	
50 Ω input	2 ns; 20 % to 80 %
1 MΩ input	10 ns; 20 % to 80 % from 50 Ω source.

Sampler and Timing

Gate Width	1 ns to 30 µs in 1-3-10 sequence, switch selectable with a continuously variable ×1 to ×5 multiplier
Sample Correlation	Less than 0.5% of the sample output due to trigger *t* remains at trigger *t* + 1
Gate Delay	
Input	0 to 10 V DC varies delay by 0.5 % to 100 % of range setting
Max delay	3 ns to 300 ns in 1-3-10 sequence plus user options, which give 10 µs (default), and 1 µs, 100 µs, 1 ms or 3 ms by capacitor change.
Trigger Source	
Internal	0.5 Hz to 40 kHz selectable with range switches 0.5, 5, 50, 500 5000, off. Vernier is 10× range.
External	
ECL	Positive edge, 5 ns min pulse width with termination of 50 Ω to -2 V; -5 V to +10 V pk-pk safe input.
TTL	Positive edge, 20 ns min pulse width; -5 V to +10 V safe input.
Max. Trigger Rate	80 kHz
Trigger Indicator	LED lights when unit is triggered
Trigger Generator	
Output	BNC TTL out on rear panel active in all trigger modes. Polarity set by jumper.
Frequency ranges	0.5, 5, 50, 500 Hz, 5 kHz and OFF with vernier to overlap ranges.
Baseline Input	TTL line to indicate whether sample is signal or baseline value.

Analog Output Averager

Mode	Linear or Exponential
Averager Reset	Front-panel push button or ground applied to **RESET AVG I/O** rear-panel input
Samples Averaged	1, 3, 10, 30, 100, 300, 1k, 10k
LSO Droop Rate	< 0.2 % FS/s
Averager Droop Rate	When there are no triggers the droop rate is < 0.001 % per minute for 10k samples

Outputs

Average Out	±10 V FS with 50 Ω output impedance and capable of driving 2 kΩ load
Last Sample Out	±10 V FS
Gate Monitor	0.3 V into 50 Ω to ground. Marker pulse-width equals gate width. Position is within 5 ns of actual gate

Internal Oscillator	TTL
Baseline Output	TTL output line that toggles with each trigger to indicate whether next sample is signal or baseline value.

General

Power Requirements	
	+24 V at 200 mA; -24 V at 150 mA +12 V at 300 mA; -12 V at 590 mA +6 V at 160 mA; -6 V at 630 mA
Dimensions	
Height	8¾" (222 mm)
Width	2¾" (70 mm)
Depth	9¾" (248 mm)
Weight	3 lb (1.4 kg)

Model 4161A Dual Channel ADC & Display Module

General

Two-channel ADC mounted in NIM enclosure with signal and trigger inputs and with trigger holdoff output. RS232 and GPIB (IEEE488) control. Separate analog edge-indicating panel meter.

Input

Channels	Two
ADC Inputs	BNC front-panel connectors, A and B
Input Impedance	1 MΩ
Input Full-Scale	±10 V
Accuracy	±5 mV
Linearity	±5 mV
ADC Trigger Inputs	BNC front-panel connectors, corresponding to channel A and channel B ADC inputs. Connectors are duplicated on rear panel
Trigger Thresholds	TTL. Triggers on rising edge of applied positive logic TTL pulse

Digital Display

Type	3½ digit LED display showing (Measured voltage / 20)
Display Selection	Switch selects channel A or channel B

Computer Interfaces

RS232	DIP switch selectable baud rate, terminator, character echo, parity and data bits.
GPIB	DIP switch selectable address and terminator
Status Indicators	Front panel LEDs indicate GPIB Talk, Listen, SRQ and Remote
Command Set	Seventeen mnemonic type commands allowing both asynchronous and synchronous readings. Digitized voltages are reported back to the computer in integer format, with ±2048 corresponding to an input voltage of ±10.24 V
Software	LabVIEW driver software suitable for version 4.01 and later of LabVIEW is available by download from our website at **www.signalrecovery.com**

Output

Busy Out

Rear-panel BNC connector generating TTL signal which under computer control will:-

1) Remain at logic 0 until a synchronized read command is issued by the computer.
2) Go to logic 1, releasing external trigger hold-off circuitry (such as can be provided by the ***SIGNAL RECOVERY*** model 9650A)
3) Return to logic 0 on receipt of a trigger signal at either the A or B ADC trigger inputs, and remain there while the measured value(s) are transferred back to the computer and thereafter until the next synchronized read command.

Analog Panel Meter

Type	Edge-indicating meter monitoring the voltage at the associated front-panel analog input BNC connector. This meter is completely independent of the analog to digital converter functions.
Input Impedance	10 kΩ
Full-scale sensitivity	±10 V

General

Power Requirements	
	+24 V at 50 mA;
	-24 V at 50 mA
	+12 V at 600 mA;
	-12 V at 30 mA
	+6 V at 550 mA;
	-6 V at 10 mA
Dimensions	
Height	8¾" (222 mm)
Width	2¾" (70 mm)
Depth	9¾" (248 mm)
Weight	2½lb (1.14 kg)

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WARRANTY

AMETEK SIGNAL RECOVERY, a part of AMETEK Advanced Measurement Technology, Inc, warrants each instrument of its own manufacture to be free of defects in material and workmanship for a period of ONE year from the date of delivery to the original purchaser. Obligations under this Warranty shall be limited to replacing, repairing or giving credit for the purchase, at our option, of any instruments returned, shipment prepaid, to our Service Department for that purpose, provided prior authorization for such return has been given by an authorized representative of AMETEK Advanced Measurement Technology, Inc.

This Warranty shall not apply to any instrument, which our inspection shall disclose to our satisfaction, to have become defective or unusable due to abuse, mishandling, misuse, accident, alteration, negligence, improper installation, or other causes beyond our control. This Warranty shall not apply to any instrument or component not manufactured by AMETEK Advanced Measurement Technology, Inc. When products manufactured by others are included AMETEK Advanced Measurement Technology, Inc equipment, the original manufacturers Warranty is extended to AMETEK Advanced Measurement Technology, Inc customers. AMETEK Advanced Measurement Technology, Inc reserves the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

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SHOULD YOUR EQUIPMENT REQUIRE SERVICE

A. Contact your local AMETEK SIGNAL RECOVERY office, agent, representative or distributor to discuss the problem. In many cases it may be possible to expedite servicing by localizing the problem to a particular unit or cable.

B. We will need the following information, a copy of which should also be attached to any equipment which is returned for service.

1. Model number and serial number of instrument
2. Your name (instrument user)
3. Your address
4. Address to which the instrument should be returned
5. Your telephone number and extension
6. Symptoms (in detail, including control settings)
7. Your purchase order number for repair charges (does not apply to repairs in warranty)
8. Shipping instructions (if you wish to authorize shipment by any method other than normal surface transportation)

C. If you experience any difficulties in obtaining service please contact:

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AMETEK Advanced Measurement Technology, Inc
801 South Illinois Avenue
Oak Ridge
TN 37831-2011, USA

Phone: +1 865 483 2121
Fax: +1 865 483 0396
E-mail: service@signalrecovery.com

or

SIGNAL RECOVERY Service
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